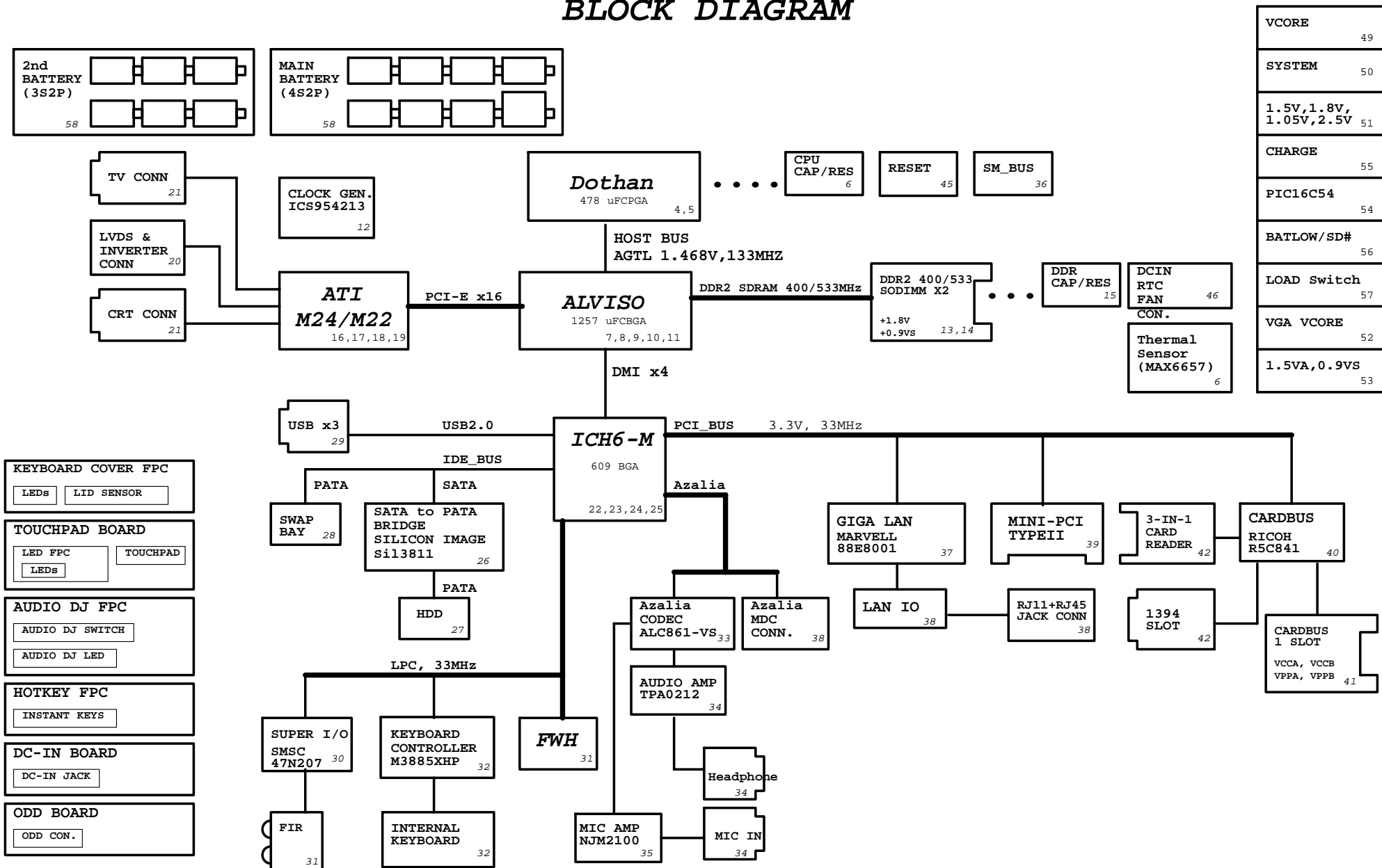


W3V/A SCHEMATIC V2.1

PAGE	Content	PAGE	Content	
	SYSTEM PAGE REF.		POWER PAGE REF.	
4	DOTHAN CPU-1	49	VCORE_MAX1987	
5	DOTHAN CPU-2	50	SYSTEM	
6	CPU CAP/THERMAL SENSOR/ITP	51	1.5V,1.8V,2.5V,1.05V	
7	ALVISO: CPU	52	VGA VCORE	
8	ALVISO: DDR2 & DMI & PEG	53	1.5VA & DDR2	
9	ALVISO: DDR2	54	PIC16C54/BATCON/PWOK	
10	ALVISO: POWER & Caps	55	CHARGER	
11	ALVISO: GND & NCTF & Straps	56	BATLOW/SD#	
12	CLOCK GEN (ICS954213)	57	LOAD SWITCH	
13	DDR2 SODIMM(0) & Caps	58	BATCON	
14	DDR2 SODIMM(1) & Caps	59	Power Flowchart	
15	DDR2 TERMINATOR	60	HISTORY	
16	ATI M24: MAIN	61	DC_IN CONN.	
17	ATI M24: MEMORY/SS	62	ODD CONN.	
18	ATI M24: PWR & GND	63	TP&LED CONN	
19	ATI M24: Strapping			
20	LVDS/INVERTER			
21	CRT/TV/TPM CONN			
22	ICH6: SATA/LPC/IDE/ACZ (1)			
23	ICH6: PCI/DMI/USB/PCIE(2)			
24	ICH6M: PWR/GND/CAPS(3)			
25	ICH6: PULL UP & Straping			
26	SATA to PATA BRIDGE			
27	HDD CON			
28	SWAP BAY CON			
29	USB PORTS			
30	SUPER I/O (LPC47N207)			
31	FIR & FWH			
32	KBC 38857			
33	Azalia AUDIO (ALC861-VS)			
34	AUDIO AMP/JACKS			
35	MIC AMP			
36	SMBUS			
37	PCI GIGA LAN (88E8001)			
38	RJ11_RJ45/MDC/BT			
39	MINIPCI			
40	PCI CARDBUS (R5C841)			
41	PCI PCMCIA SOCKET A			
42	IEEE1394A/3in1 CONN			
43	LEDs & DEBUG PORT			
44	DJ/HOTKEY/TP LED			
45	PWR SW/RESET/KBC LED			
46	FAN & DC_IN			
47	POWER-ON SEQUENCE			
48	DISCHARGE/EMI/VCCA			

W3V/A:Dothan & Alviso-PM+M24-CSP/Alviso-GM BLOCK DIAGRAM



bom



PROJECT: W3V

REVISION
2.1

DATE: Monday, January 17, 2005
SHEET 2 OF 63

DESCRIPTION:
BLOCK DIAGRAM

SCHEMATIC FILE NAME :
RELEASE DATE :

DESIGN ENGINEER :
Alice Shih

PCI Device	IDSEL#	REQ/GNT#	Interrupts	PC/PCI
Chipset (Host to PCI)	(AD30 internal)	n/a		
Mini_PCI	AD18	3	B,D	
LAN --88E8001	AD16	0	C	
CardBus	AD17	1	B	
1394	AD17	1	A	
3 IN 1		1	C	

Azalia : PCI_INTB#
 USB 0,1 : PCI_INTA#
 USB 2,3 : PCI_INTD#
 USB 4,5 : PCI_INTC#

SMBUS ADDRESS :

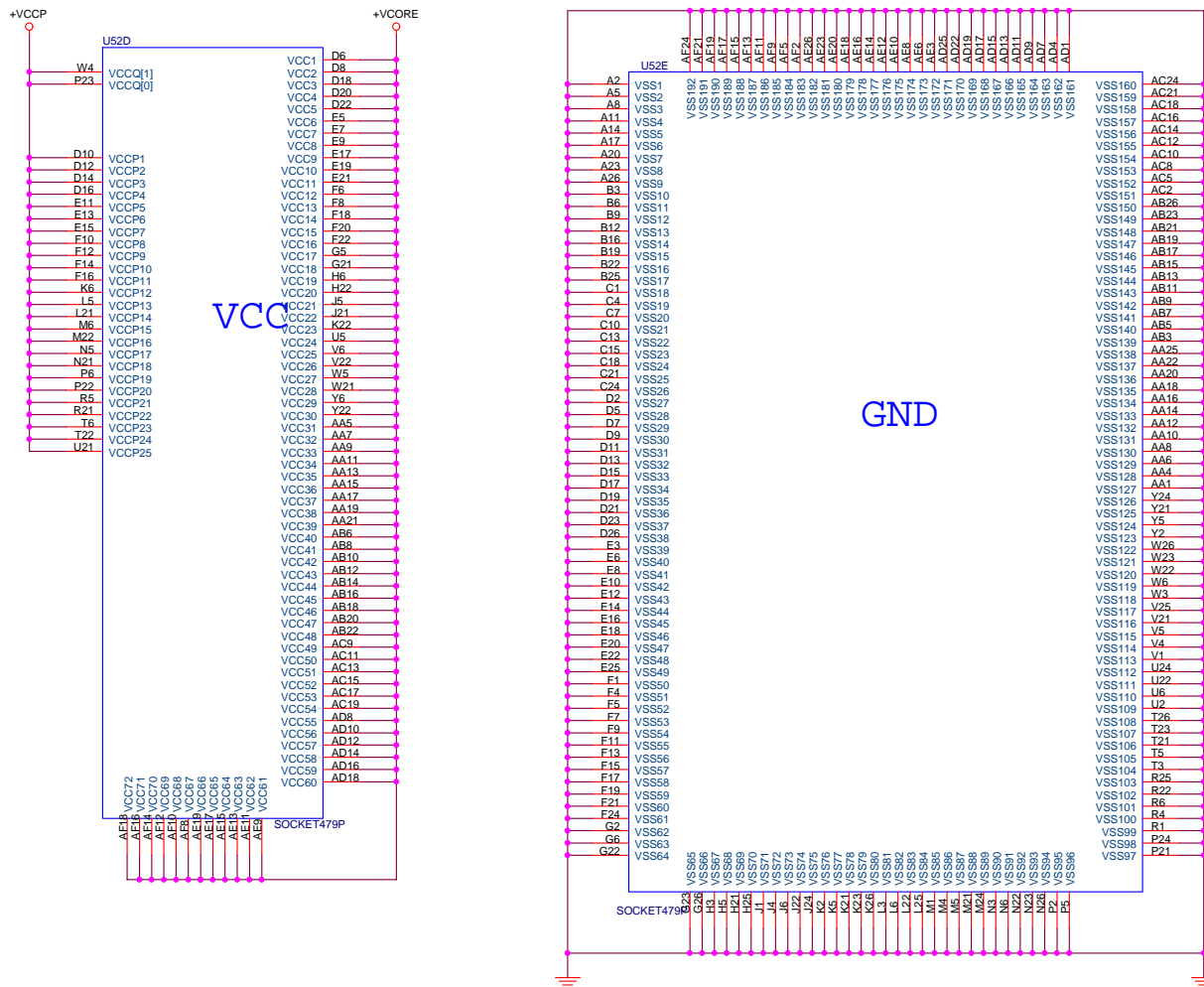
CLK = 1101001x (D2)
 DDR_SODIMM0 = 1010010x (A4)
 DDR_SODIMM1 = 1010000x (A0)
 THERMAL = 1001100x (98)

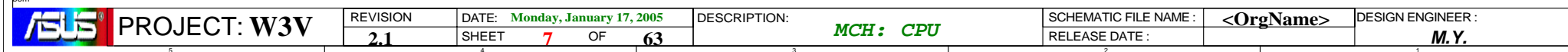
ICH6M_GPIO	Used As	Signal Name
GPI000	GPI	KBDDT0
GPI001	GPI	KBDDT1
GPI006	GPI	PM_BMBUSY#
GPI007	GPI	FIR_SEL
GPI008	GPI	EXTSMI#_3A
GPI011	GPI	LID_ICH#_3A
GPI012	GPI	KBDSOI_3
GPI013	GPI	ATI_OVERTEMP#
GPI014	GPI	GPI14
GPI015	GPI	CHG_EN#_OC
GPI016	GPO	GPO16
GPI017	GPO	GPO17
GPI021	GPO	BACK_OFF#
GPI023	GPO	FWH_WP#
GPI024	GPO	CB_SD#
GPI025	BLINK	ICH6_1HZ
GPI026	GPI	SATA_DET_#0
GPI027	GPI	PCB_VID0
GPI028	GPI	PCB_VID1
GPI029	GPI	PCB_VID2
GPI030	GPI	SATA_DET_#2
GPI031	GPI	AGP_EXT
GPI033	GPO	XIDE_EN#_3
GPI034	GPO	OP_SD#
GPI040	GPI	PID0
GPI041	GPI	PID1

M38857_GPIO	Used As	Signal Name
P20	GPO	KBCRSM
P21	GPO	BAT_SEL
P22	GPO	BAT_LEARN
P23	GPO	MSK_INSTKEY#
P42	GPO	WATCHDOG
P43	GPI	SWDJ_EN#
P44	GPO	KBCPURST_3Q
P45	GPO	KBC_GA20
P46	GPO	KBSCI_3Q
P47	GPI	PM_CLKRUN#
P50	GPI	BAT_LLOW#_KBC
P51	GPO	DJ_LED_EN
P52	GPO	WIRELESS_LED#
P53	GPO	BAT_LOW#_KBC
P54	GPI	BAYDOCK_IN#
P55	GPI	BAT1_IN#_OC
P56	GPO	FAN_DA
P57	GPO	ADJ_BL
P60	GPI	BT_#
P61	GPI	INTERNET_#
P62	GPI	CPUFAN_SPD_A
P63	GPI	WIRELESS_#
P64	GPI	ACIN_OC
P65	GPI	MARATHON_#
P66	GPO	PANLOCK_#
P67	GPI	BAT2_IN#_OC
P76	GPI	SMD_BAT_KBC
P77	GPO	SMC_BAT_KBC

M38857_GPIO	Used As	Signal Name
P27	GPO	--
P26	GPO	NUM_LED#
P25	GPO	CAP_LED#
P24	GPO	SET_PCIRSTNS#
P41	GPO	BT_LED#
P40	GPO	KBC_EXTSMI

47N207_GPIO	Used As	Signal Name
GP10	GPI	BAY_IN0
GP11	GPI	BAY_IN1
GP12	GPI	--
GP13	GPI	SW_RST#
GP14	GPI	--
GP15	GPO	BAY_RST
GP16	GPO	DJKEY_EN
GP17	GPO	802_EN#
GP34	GPO	OVER_CLK1
GP35	GPO	OVER_CLK2
GP36	GPO	--







14 M_A_DQ[0..63]

13 M_B_DQ[0..63]

DDR SYSTEM MEMORY A

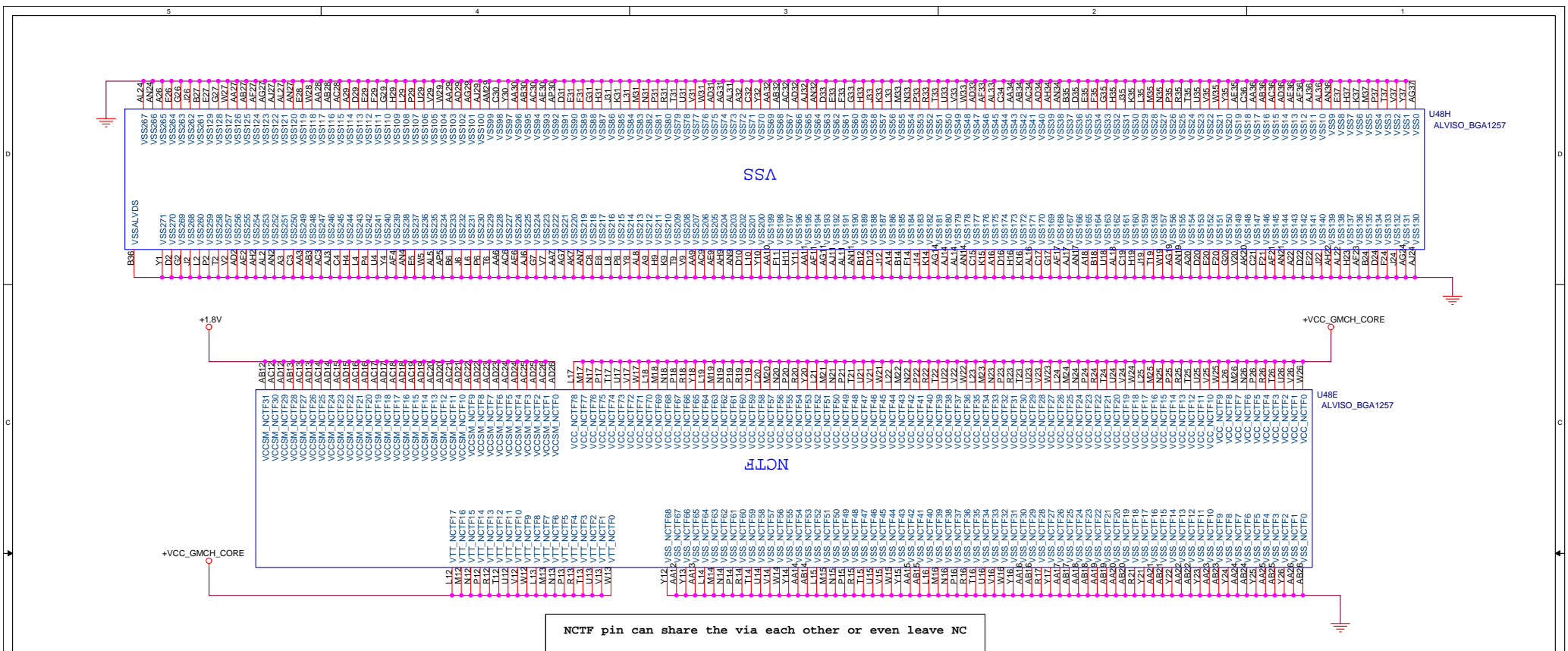
DDR SYSTEM MEMORY B

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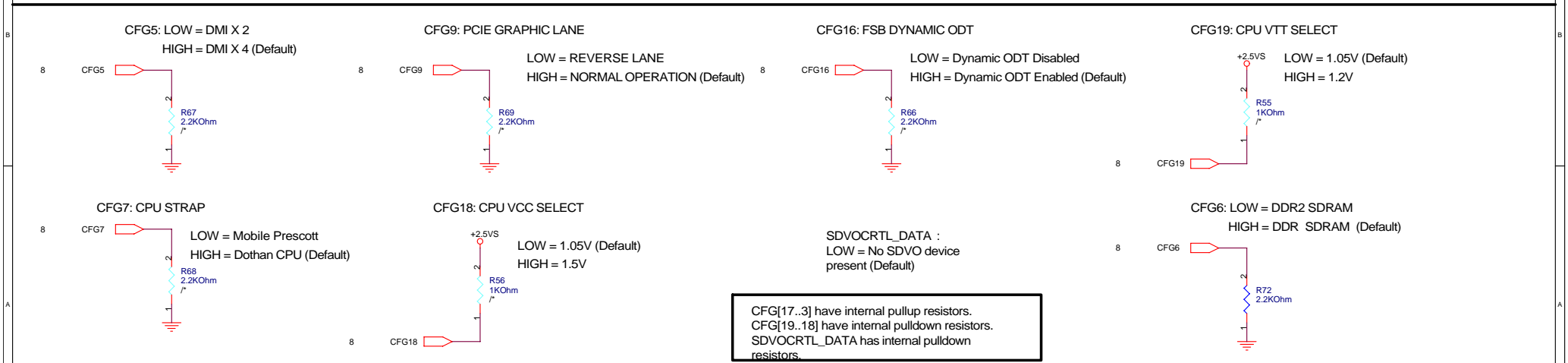


PROJECT: W3V

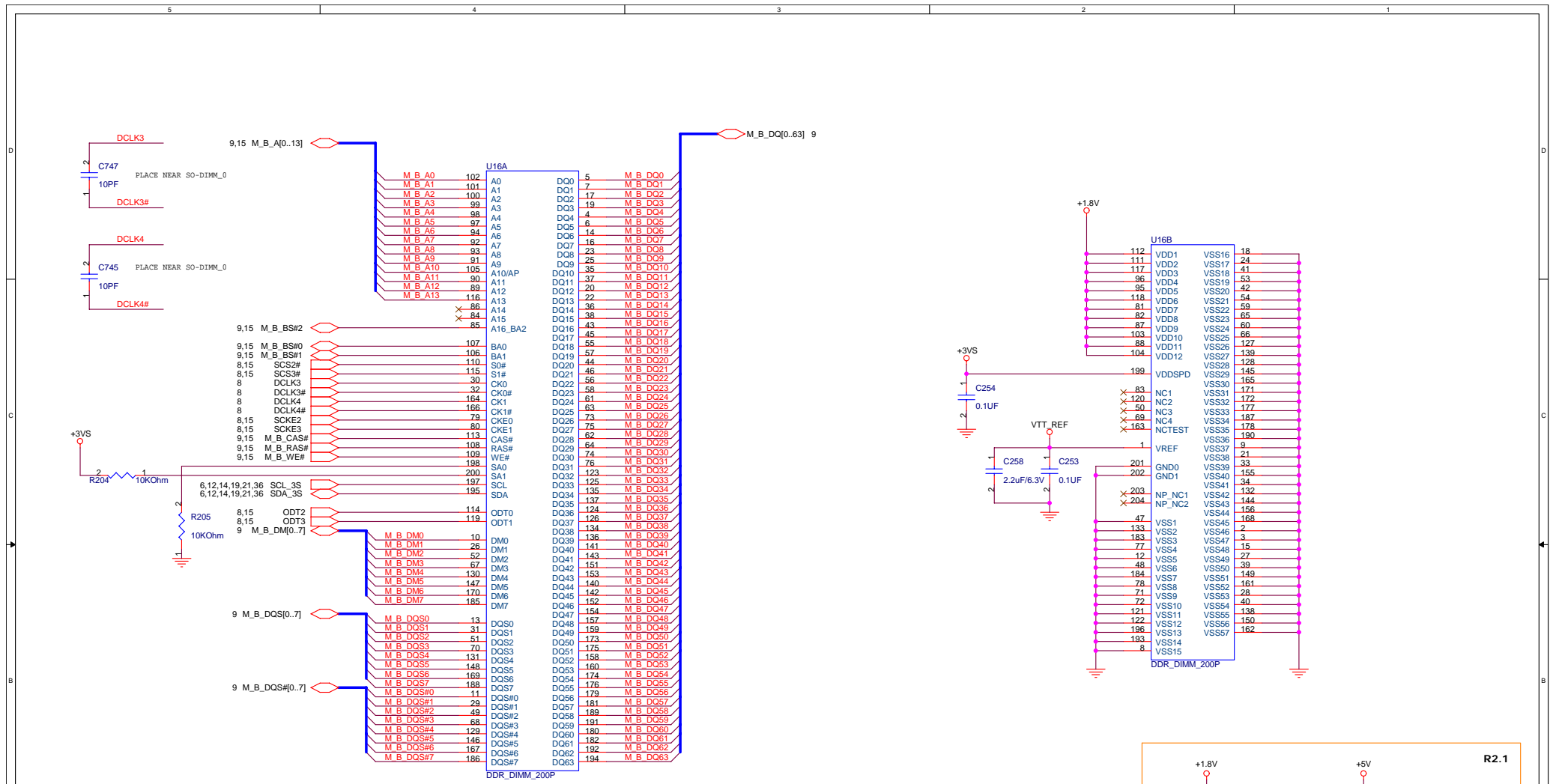
REVISION
2.1DATE: Monday, January 17, 2005
SHEET 9 OF 63DESCRIPTION:
MCH: DDR2SCHEMATIC FILE NAME : <OrgName>
RELEASE DATE :DESIGN ENGINEER :
M.Y.



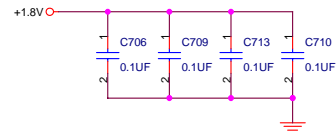
NCTF pin can share the via each other or even leave NC



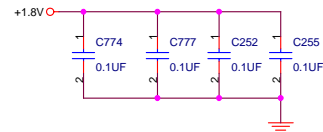




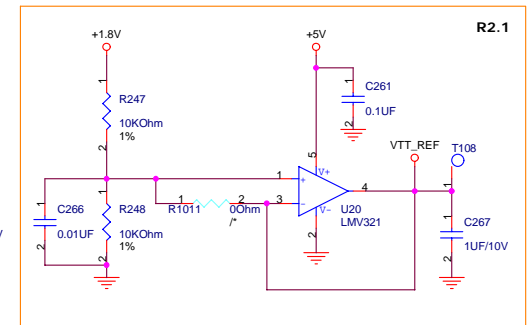
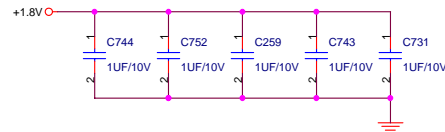
Layout Note: Place these High-Freq decoupling Caps near the GMCH



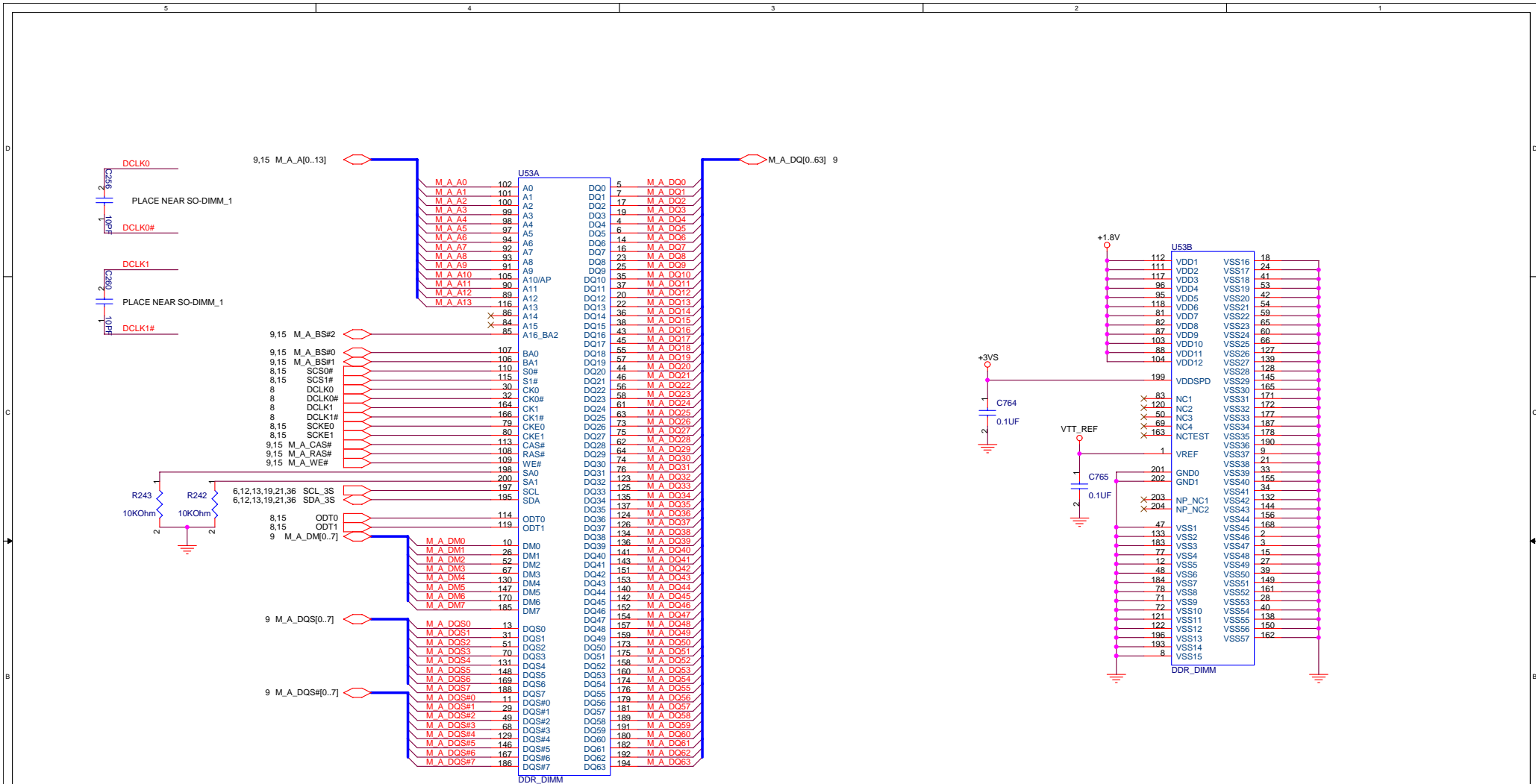
Layout Note: Place these Caps near SO DIMM 0



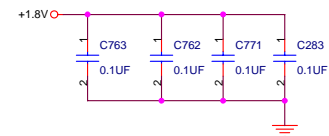
Layout Note: Place these Caps near SO DIMM 0



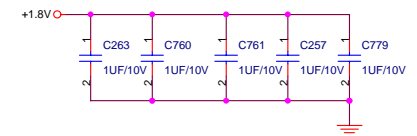
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Layout Note: Place these Caps near SO DIMM 1

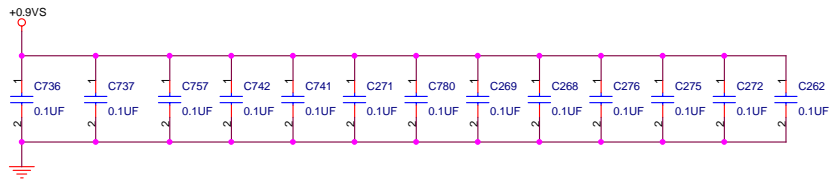
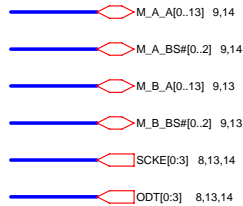
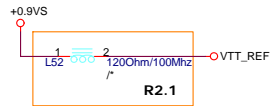


Layout Note: Place these Caps near SO DIMM 1

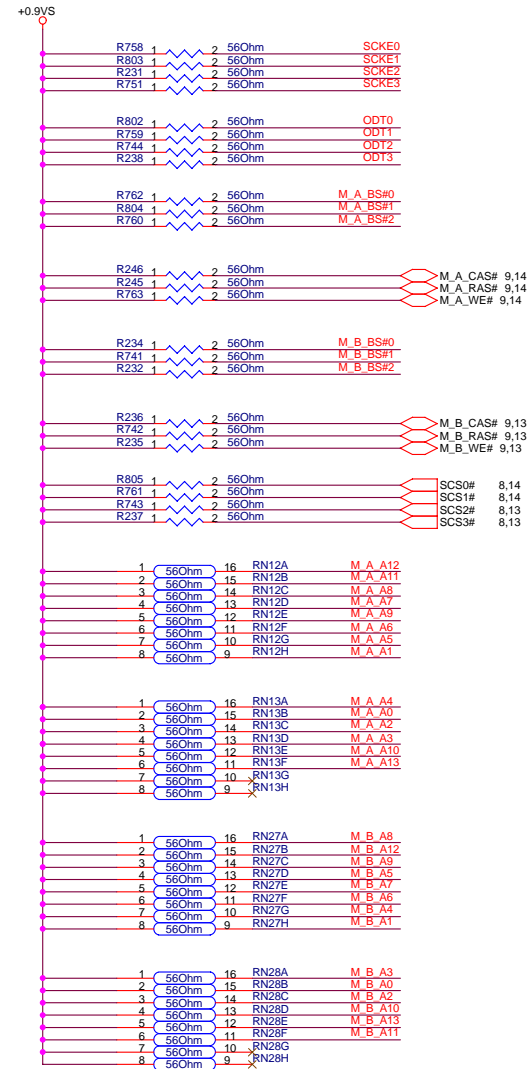
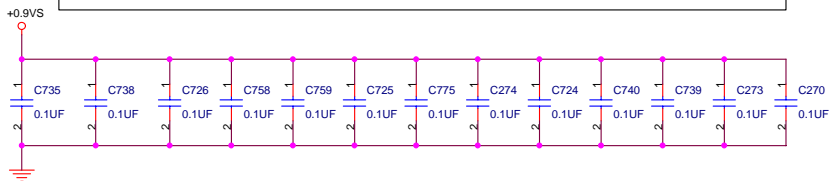


bom

	PROJECT: W3V	REVISION 2.1	DATE: Monday, January 17, 2005 SHEET 14 OF 63	DESCRIPTION: DDR2 SO-DIMM (2)	SCHEMATIC FILE NAME : RELEASE DATE :	<OrgName>	DESIGN ENGINEER : M.Y.
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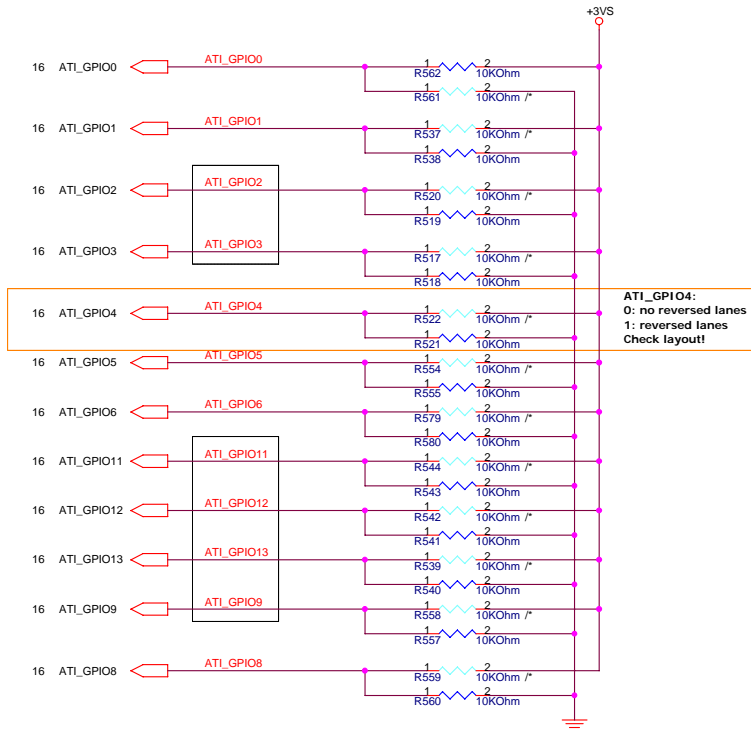


Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9VS





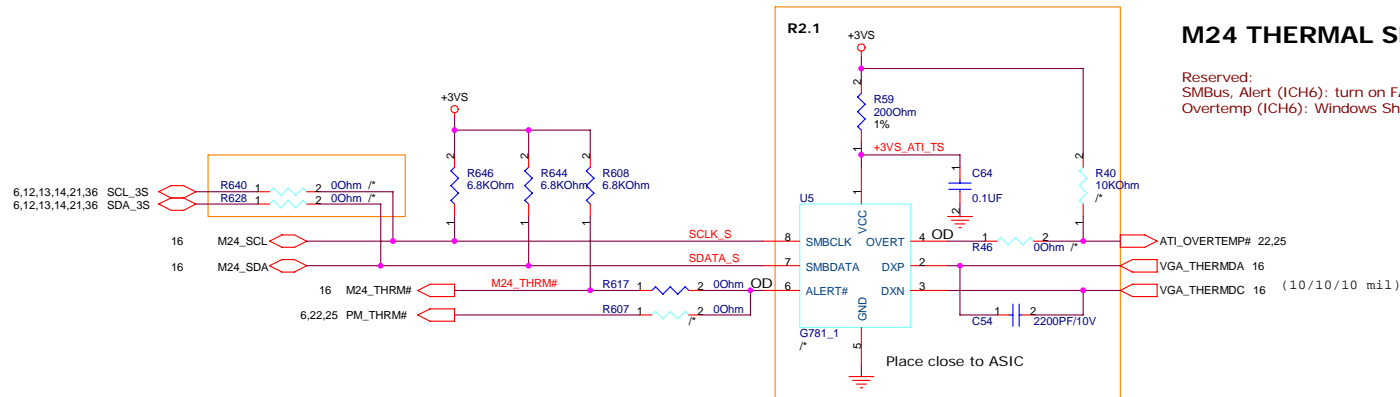
OPTION STRAPS



GPIO[0:13] : Internal PD

STRAPS	PIN	DESCRIPTION	ASIC DEFAULT
B_PRX_IDLE_MODE (for A21) B_PTX_PDNB_MODE	PCIE_TEST	(For A21) PHY Receiver Idle Detector 0: Normal idle detector / 1: Alternate idle detector ATI internal use only. Other logic must not affect this signal during RESET	0
B_PTX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (recommended) Must have an external 10K pullup to 3.3V	0
B_PTX_DEEMPH_EN	GPIO1	Transmitter De-emphasis Enable 0: Tx de-emphasis disable for mobile mode 1: Tx de_emphasis enable	0
PCIE_MODE(1:0)	GPIO(3:2)	00: PCI Express 1.0A mode 01: Kyrene-compatible mode 10: PCI Express 1.0 mode 11: PCI Express 1.0A mode and short-circuit internal loopback mode (Rx connected directly to Tx of PHY)	00
B_PTX_IEXT (For M24 A21/M22 A11)	GPIO4	0: normal mode 1: extra current in Tx output stage	0
REVERSE LANES (For M24A23/M22 A13)		0: non-reversed lanes layout 1: reversed lanes layout	0
FORCE_COMPLIANCE	GPIO5	Force chip to go to compliance state quickly for test purposes	0
B_PLL_BW (For M24 A21/M22 A11)	GPIO6	0: Full PLL Bandwidth 1: Reduced PLL Bandwidth (ATI internal use only. Other logic must not affect this during RESET.)	0
CM_RANGE (For M24A23/M22 A13)		0: normal common-mode range 1: extended common-mode range	0
DEBUG_ACCESS	GPIO8	Controls whether ROM bytes 77-76 are used as SUBSYS_VEN_ID strap or DEBUG_PORT_MUX_SELECT strap.	0
ROMIDCFG(3:0)	GPIO(9,13:11)	If no ROM attached, controls chip IDis. If ROM attached identifies ROM type 00x - No ROM, CHG_ID=0 0x1x - No ROM, CHG_ID=1 1000 - Parallel ROM, chip IDis from ROM 1001 - 1M Serial AT25F1024 ROM (Atmel) 1010 - 1M Serial AT45DB011 ROM (Atmel) 1011 - 1M Serial M25P10 ROM (ST) 1100 - 512K Serial M25P05 ROM (ST) 1101 - 1M Serial SST45LF010 (SST), W45B512 (Winbond), 512K W45B012 (Winbond) 1110 - 1M SST25VF010 (SST), 512K SST25VF512 (SST) 1111 - 1M Serial NX25F011B (NextFlash)	0000 (internal PD)
VIP_DEVICE	DVPDATA_20	0: Slave VIP host port device present 1: No slave VIP host port device	(internal PD)
PKGTTYPE(4:0)	DVPDATA(15:11)	ATI internal use only Identifies package/memory combinations	

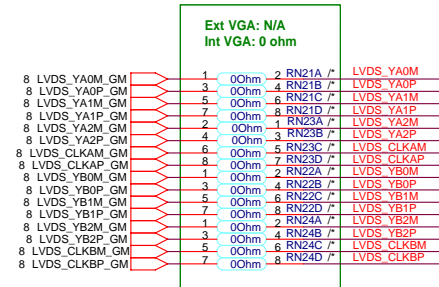
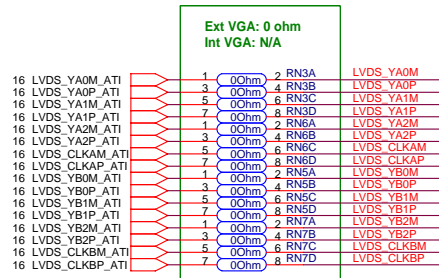
M26: GPIO11 is memory aperture size (0=128M, 1=256M)



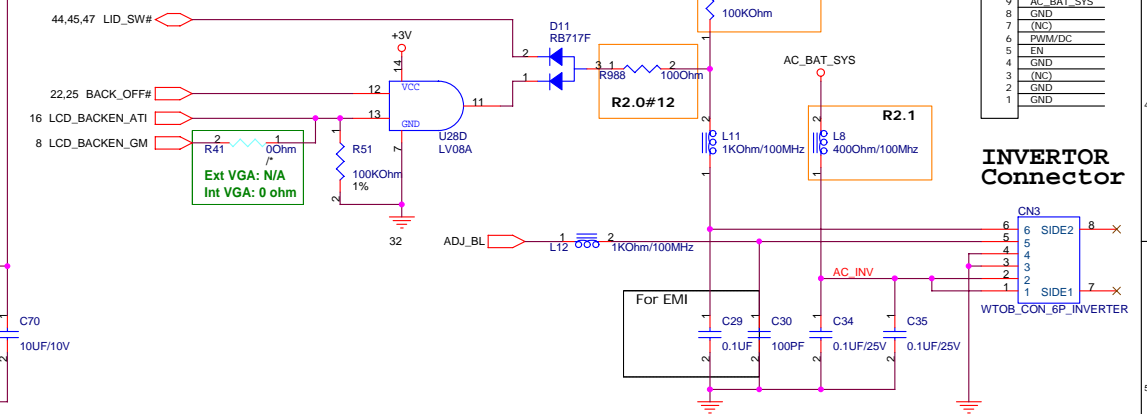
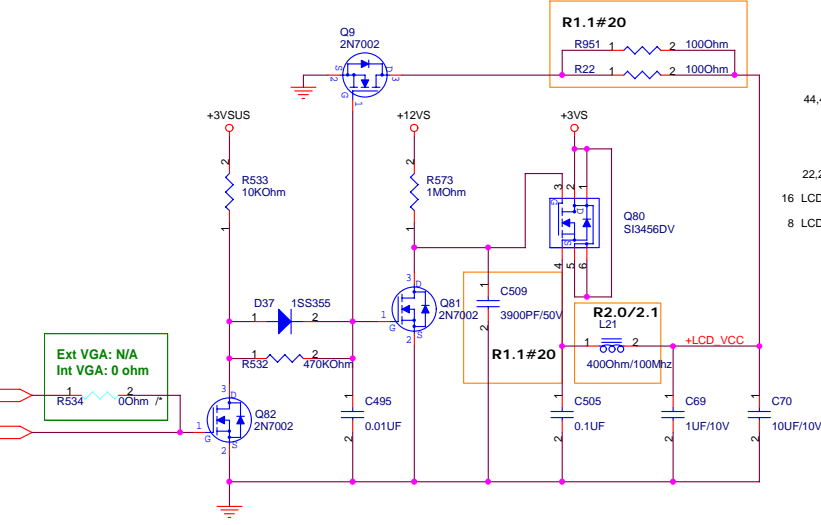
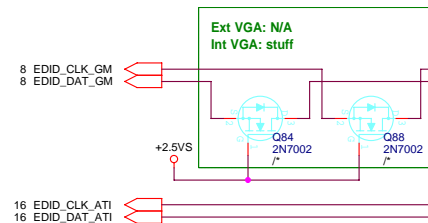
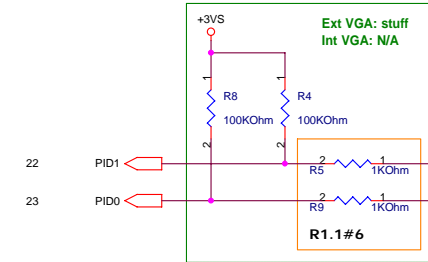
M24 THERMAL SENSOR

Reserved:
SMBus, Alert (ICH6): turn on FAN
Overtemp (ICH6): Windows Shutdown

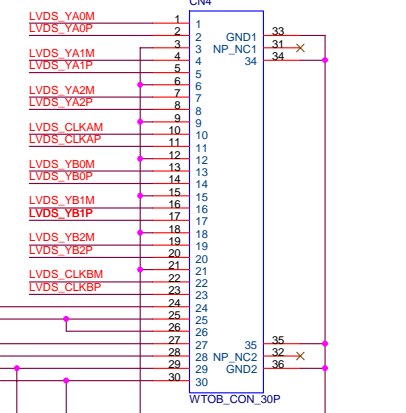
Ext VGA: stuff
Int VGA: N/A



LCD CABLE ID	PID1	PID0
14" WXGA (AU/SS/CMO/CPT)	0	0



LVDS Connector

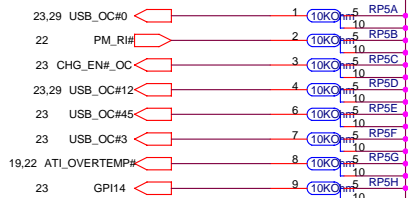
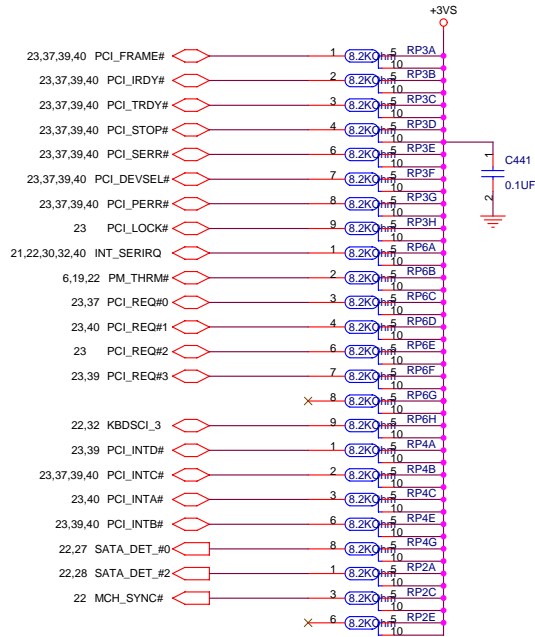


INVERTER Connector

INVERTER Connector

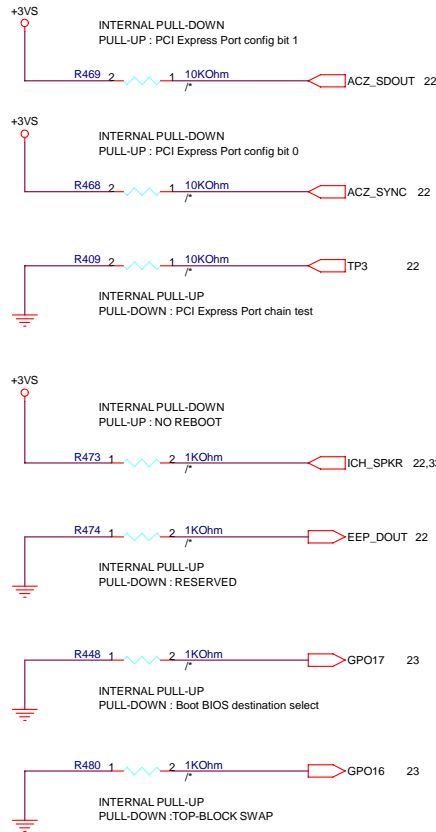
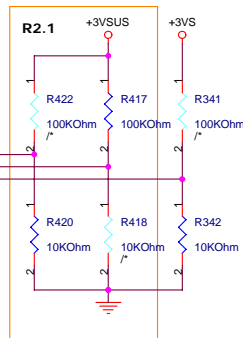






22 PCB_VID0
22 PCB_VID1
22 PCB_VID2

	PCB_VID2	PCB_VID1	PCB_VID0
MB R1.0	0	0	0
MB R1.1	0	0	0
MB R2.0	0	0	1
MB R2.1	0	1	0

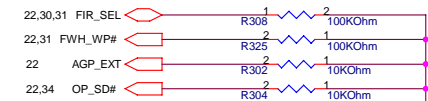
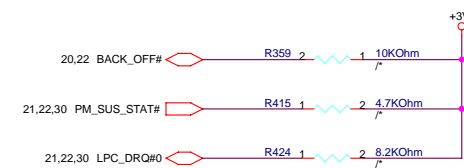
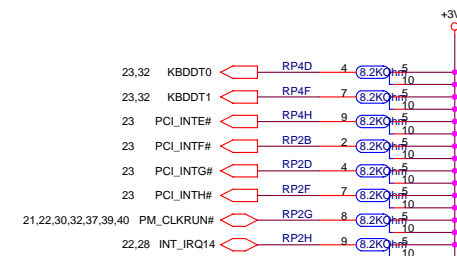
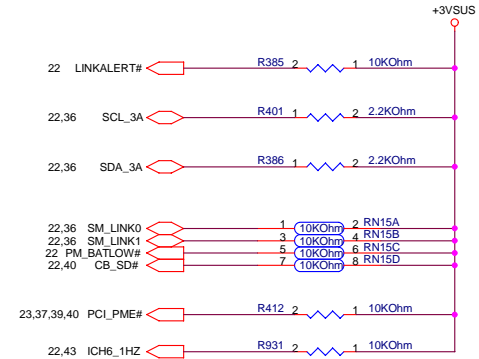


INTERNAL PULL-DOWN SIGNALS :

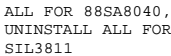
AC_BITCLK, AC_RST#, AC_SDIN[2:0],
AC_SDOUT, AC_SYNC, DPSLPVR,
LAN_CLK, PDD[7], PDDREQ, SPKR,
USB[7:0][P.N]

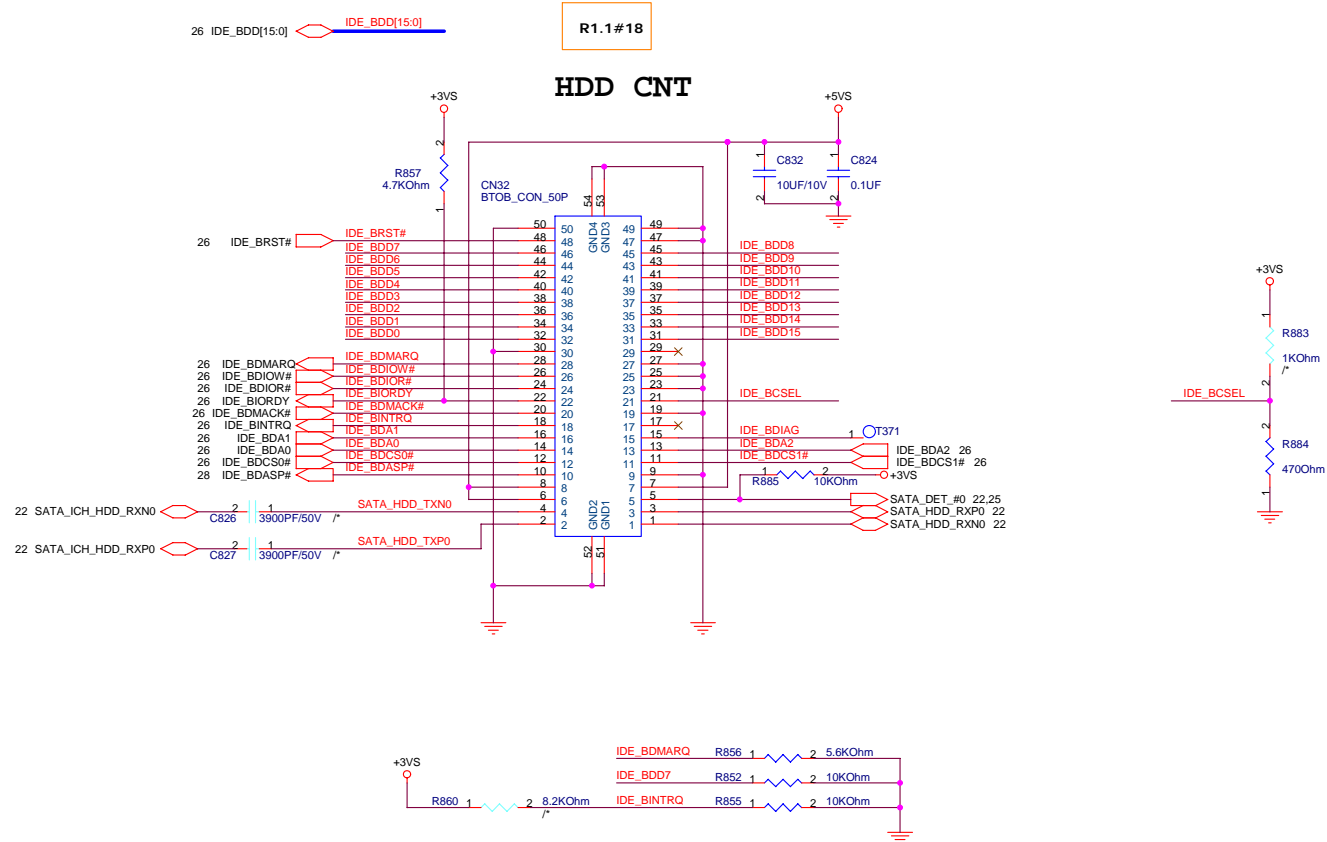
INTERNAL PULL-UP SIGNALS :

EE_DIN, EE_DOUT, EE_CS,
GPIO[17:16], LAD[3:0]#,
LDRQ[0:1], LAN_RXD[2:0],
PME#, PWRBTN#, TP3,
SATALED#,
GNT[4:0]

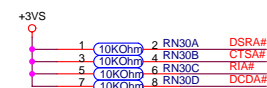
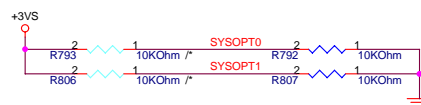
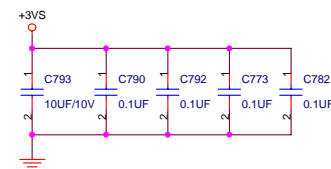


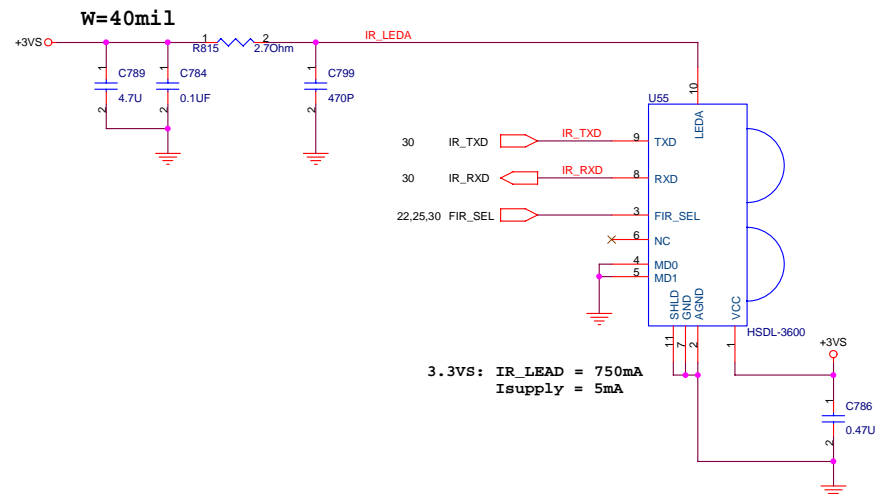
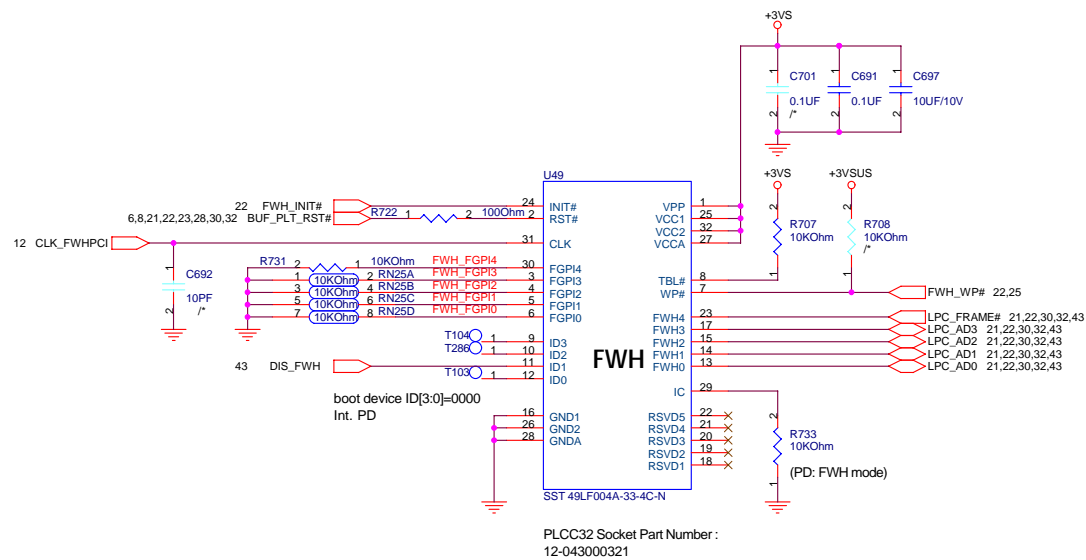
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[illegible]



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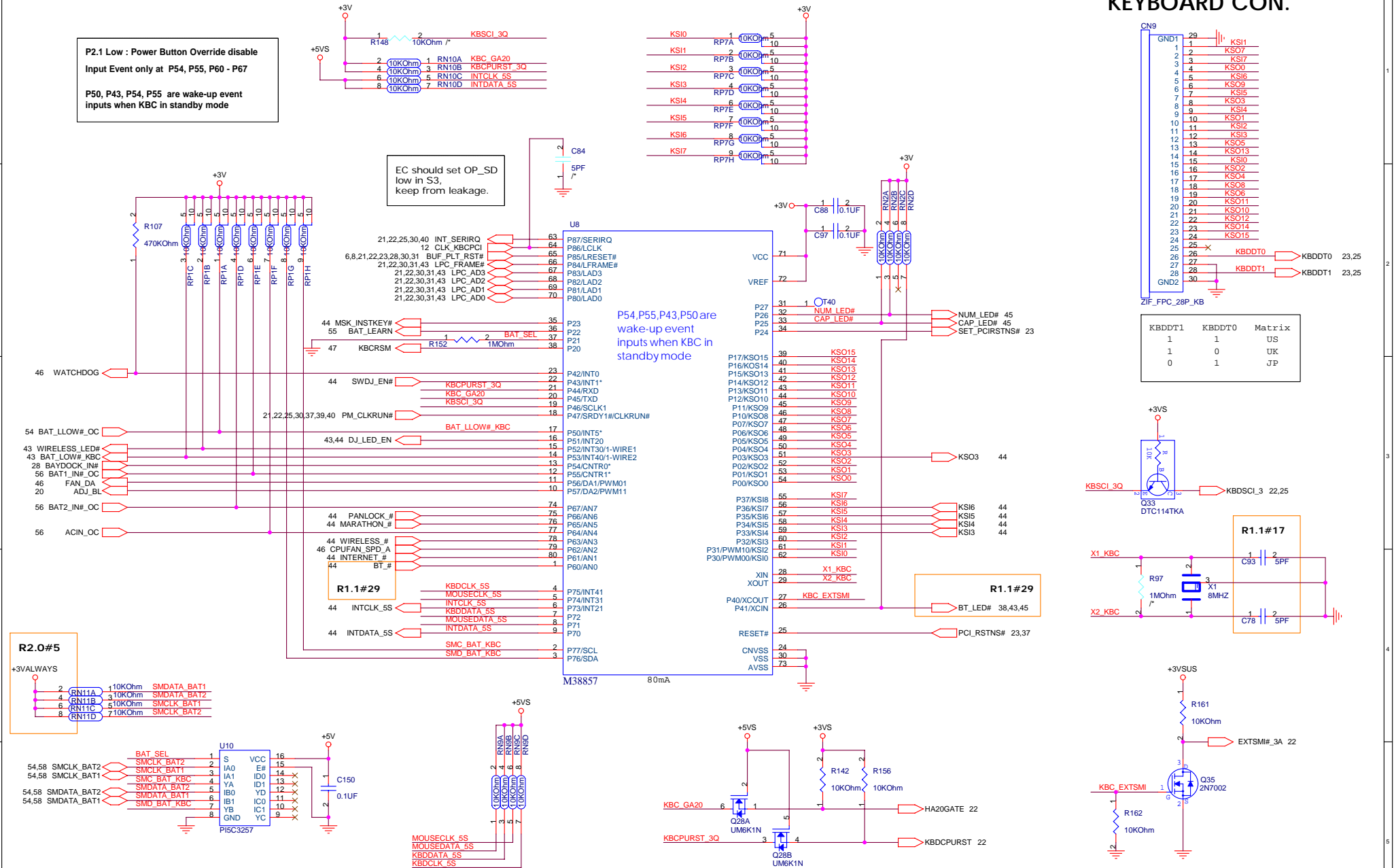
	PROJECT: W3V	REVISION 2.1	DATE: Monday, January 17, 2005 SHEET 31 OF 63	DESCRIPTION: FIR & FWH	SCHEMATIC FILE NAME : <OrgName> RELEASE DATE :	DESIGN ENGINEER : Alice Shih
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P2.1 Low : Power Button Override disable
Input Event only at P54, P55, P60 - P67
P50, P43, P54, P55 are wake-up event inputs when KBC in standby mode

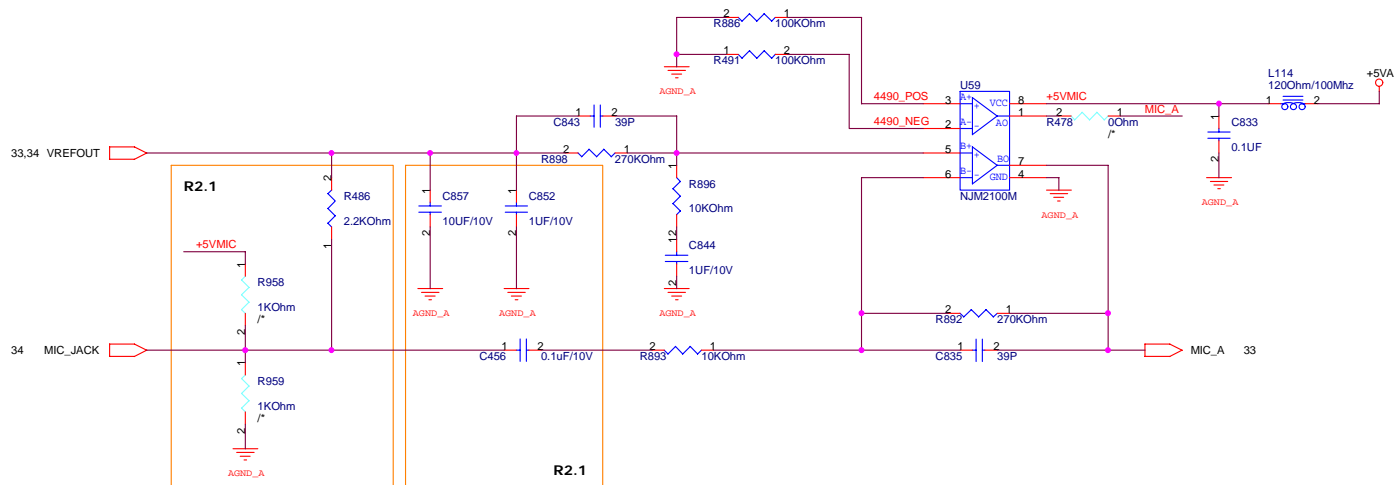
EC should set OP_SD low in S3, keep from leakage.

P54, P55, P43, P50 are wake-up event inputs when KBC in standby mode

KEYBOARD CON.

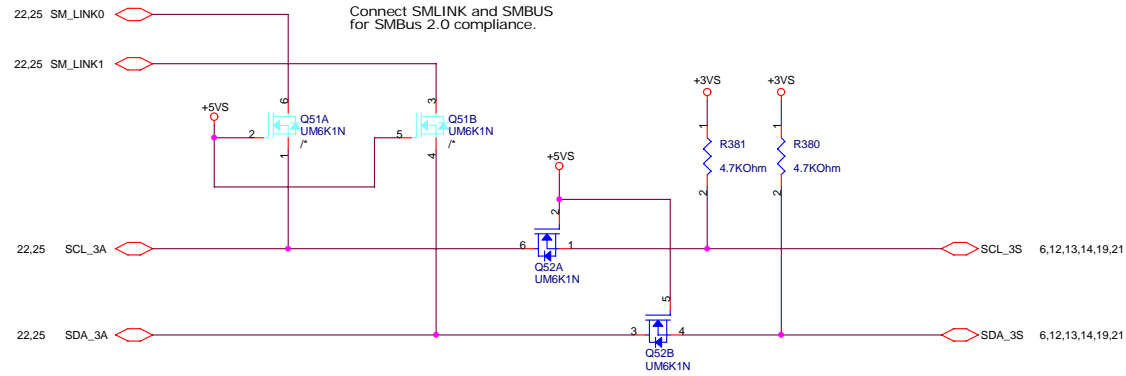






ICH6-M

ICH6-M



System Thermal Sensor
ATI Thermal Sensor
Clock Generator
DDR2 SO-DIMM
TPM

+3VALWAYS	+3VALWAYS	21,22,32,34,43,44,45,47,48,50,51,57
+3VSUS	+3VSUS	20,22,24,25,31,32,37,45,47,53,57
+5VALWAYS	+5VALWAYS	48,51,53
+5VSUS	+5VSUS	24,57
+1.5VSUS	+1.5VSUS	24,53
+3V	+3V	20,23,30,32,34,37,38,39,40,41,42,43,44,47,48,53,57
+5V	+5V	13,21,29,32,33,41,43,44,45,48,52,56,57
+12V	+12V	34,42,57
+3VS	+3VS	6,10,12,13,14,16,17,18,19,20,21,22,24,25,26,27,28,30,31,32,33,37,38,39,40,43,45,47,48,49,52,53,54,57
+5VS	+5VS	21,24,27,28,32,34,37,39,43,45,46,48,57
+12VS	+12VS	20,21,28,44,57
+VCORE	+VCORE	5,6,49
+VCCP	+VCCP	4,5,6,7,10,12,22,24,48,53
+1.2VSP	+1.2VSP	18,52
+2.5VS	+2.5VS	6,8,10,11,18,20,21,24,48,51,52
+1.8VS	+1.8VS	4,16,17,18,26,48,52,53,57
+0.9VS	+0.9VS	15,53
+1.5VS	+1.5VS	4,8,10,18,23,24,48,51
+VCC_RTC	+VCC_RTC	22,24
+1.8V	+1.8V	8,10,11,13,14,40,51,53
+VCC_GMCH_CORE	+VCC_GMCH_CORE	8,10,11,53
+VCCCB	+VCCCB	40,41
+VPPCB	+VPPCB	41
VTT_REF	VTT_REF	8,13,14,15
A/D_DOCK_IN	A/D_DOCK_IN	46,55,56
+ATI_VCORE	+ATI_VCORE	18,52

bom



PROJECT: W3V

REVISION
2.1

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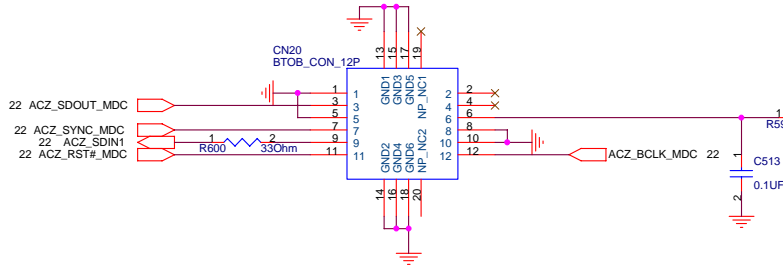
DESCRIPTION:
SMBUS

SCHEMATIC FILE NAME : <OrgName>
RELEASE DATE :

DESIGN ENGINEER :
M.Y.

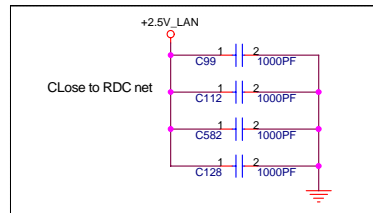
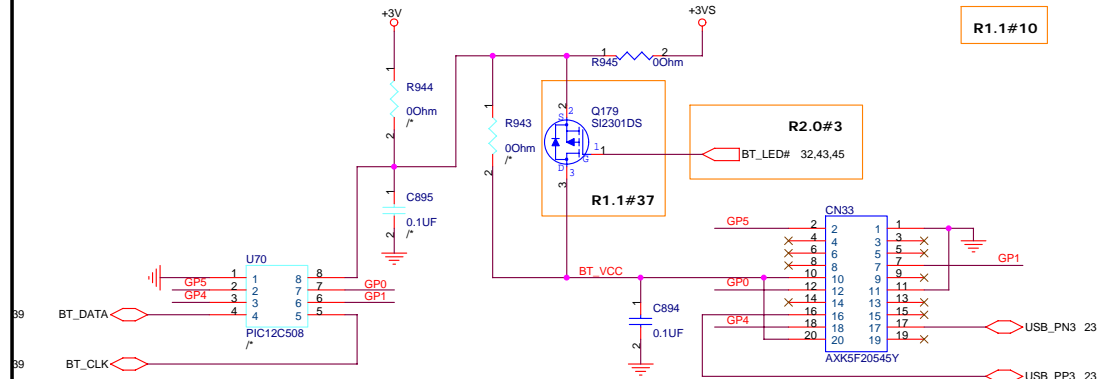
Azalia MDC MODEM

[ACZ_SDOUT/SYNC/BITCLK/RST#]:
ICH6: 39 ohm to Audio / 39 ohm to MDC
[ACZ_SDIN]:
Audio 33 ohm to ICH6 / MDC 33 ohm to ICH6



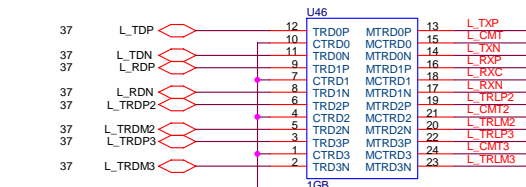
BT

R1.1#10

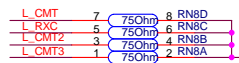


Close to RDC net

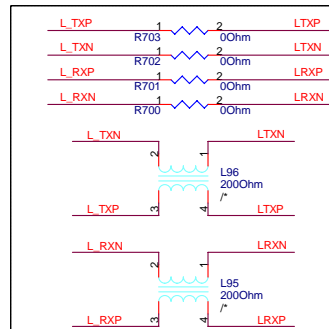
PLACE NEAR RJ45



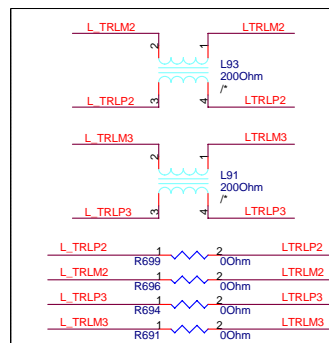
PLACE NEAR TRANSFORMER



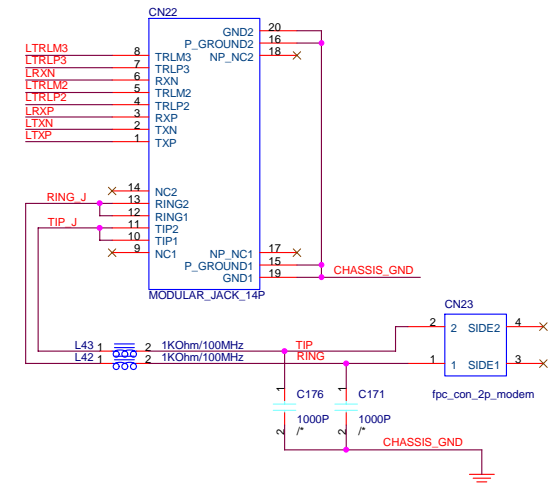
FGND1S



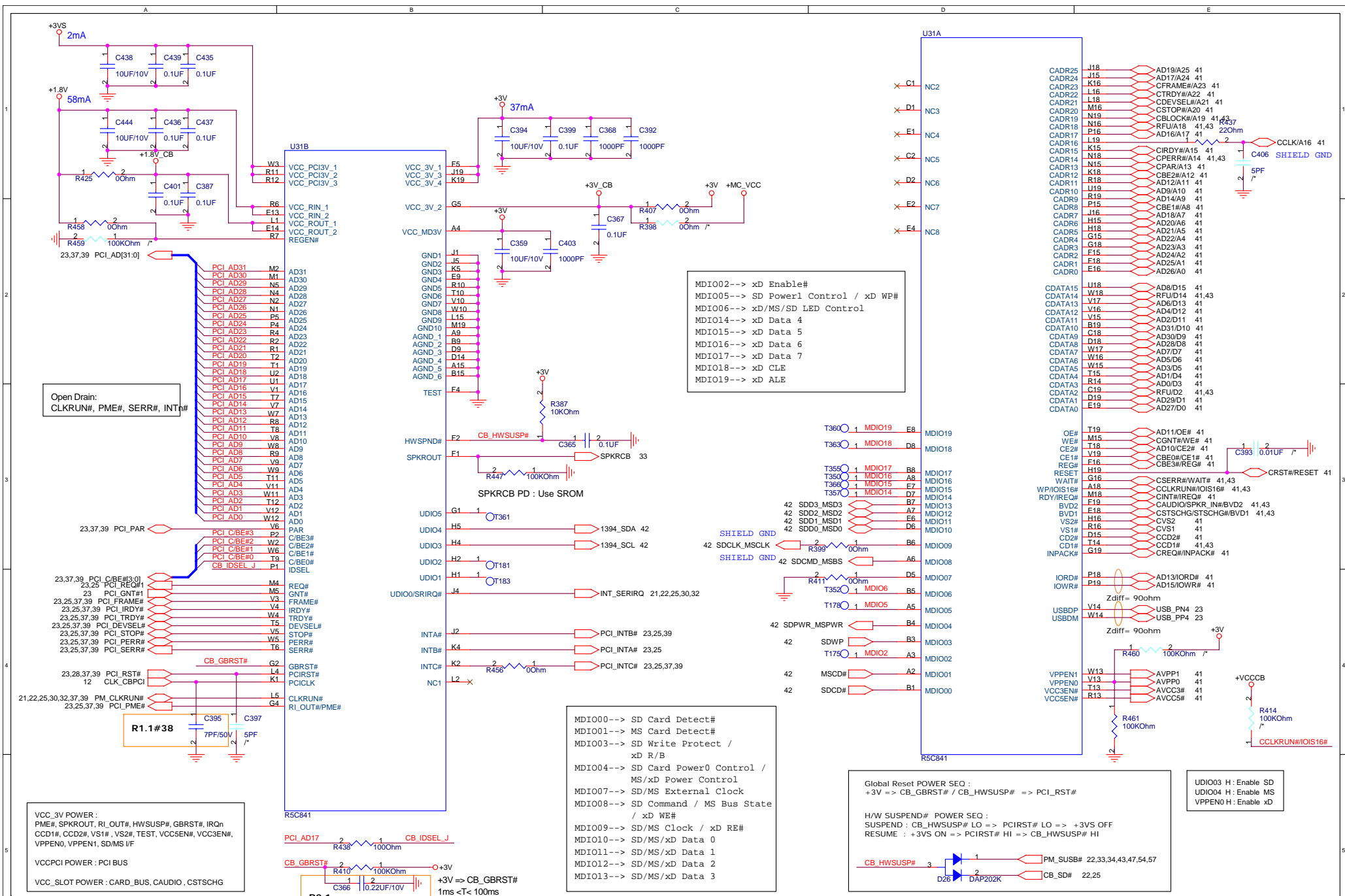
Co-Layout
Reserved for EMI



Co-Layout
Reserved for EMI

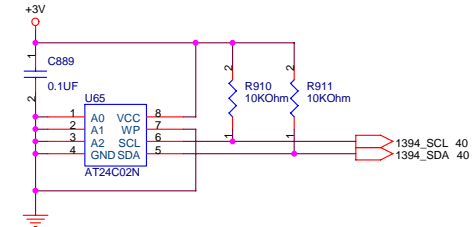
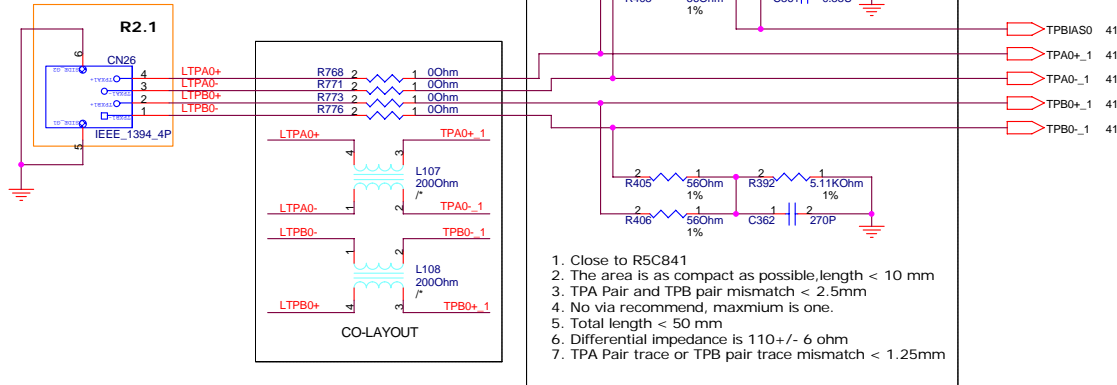


RJ11+RJ45

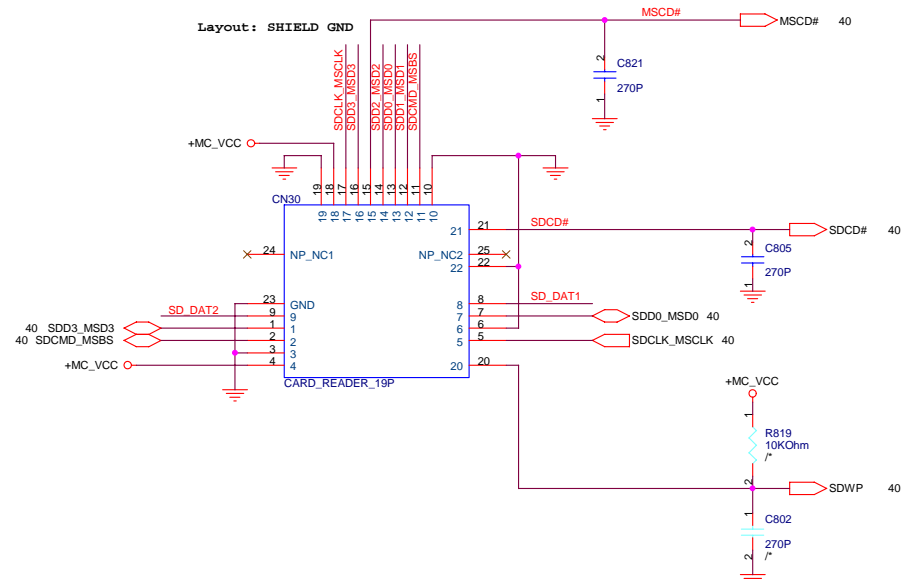
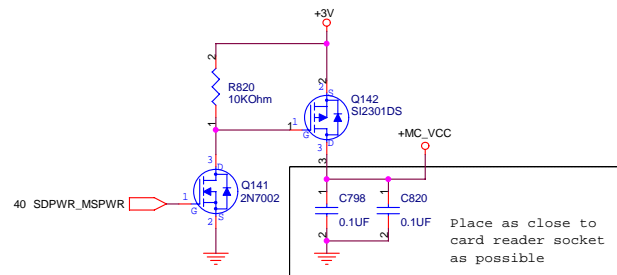
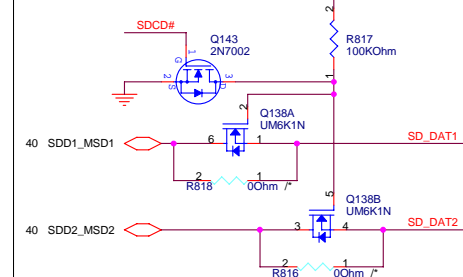




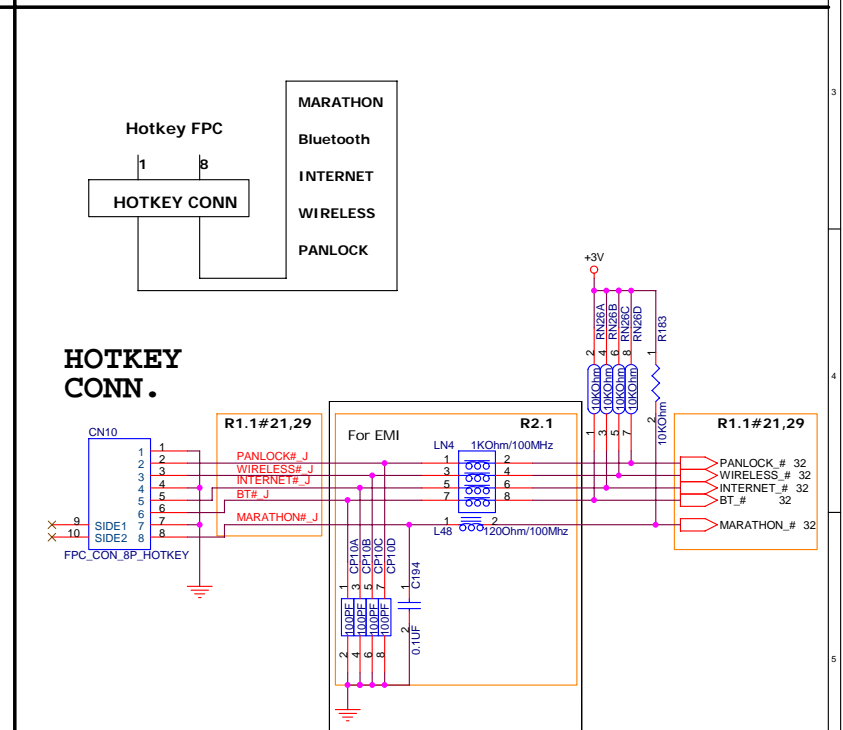
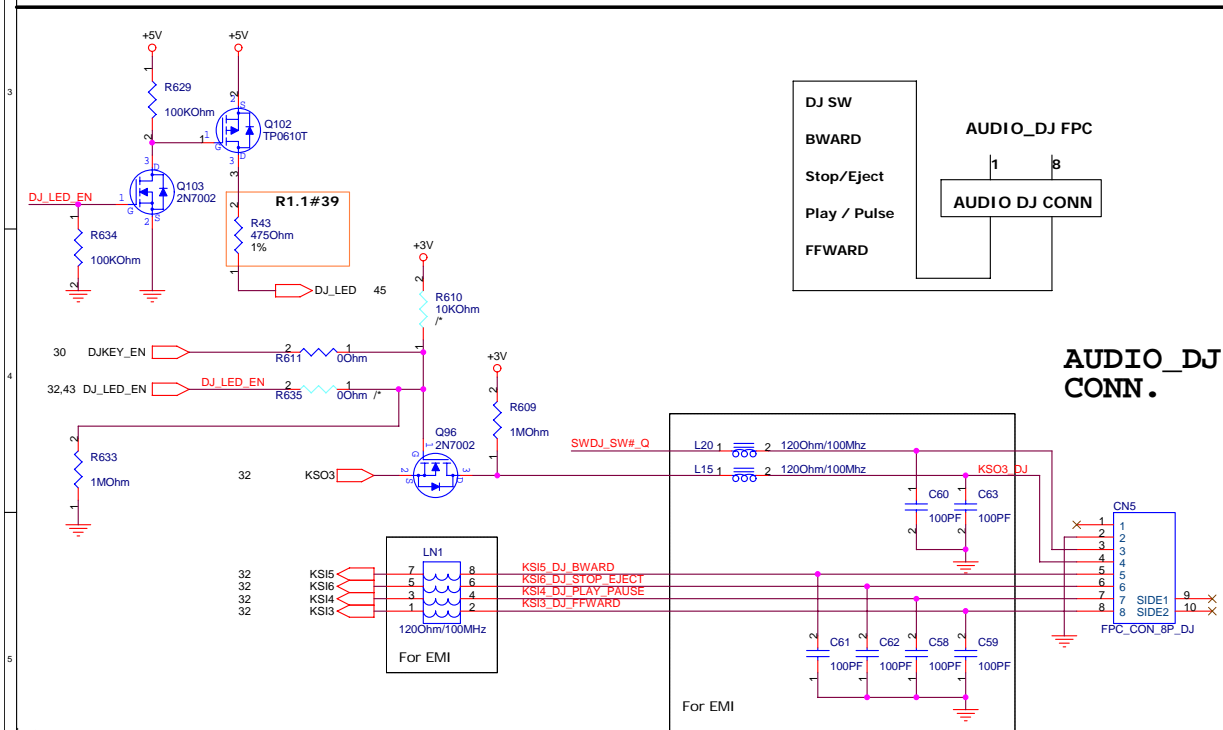
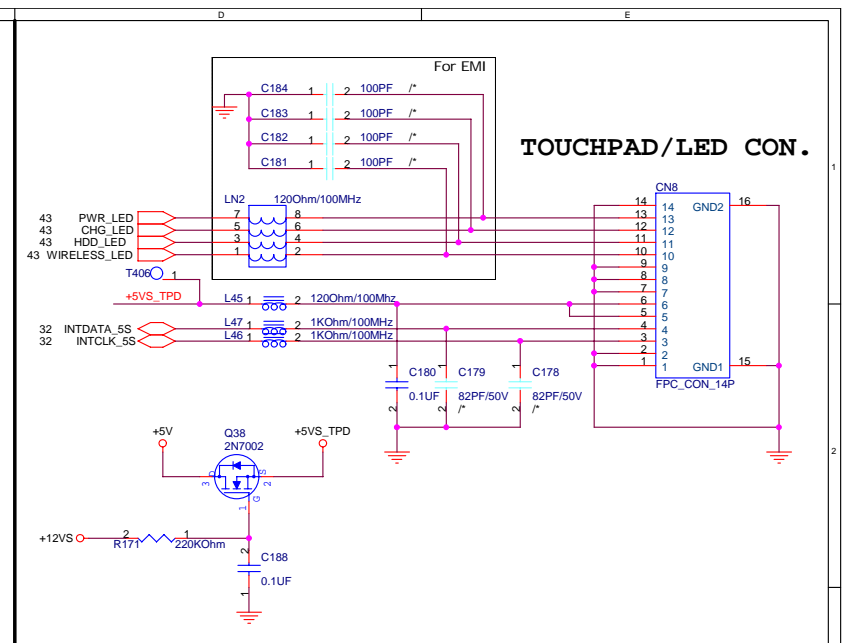
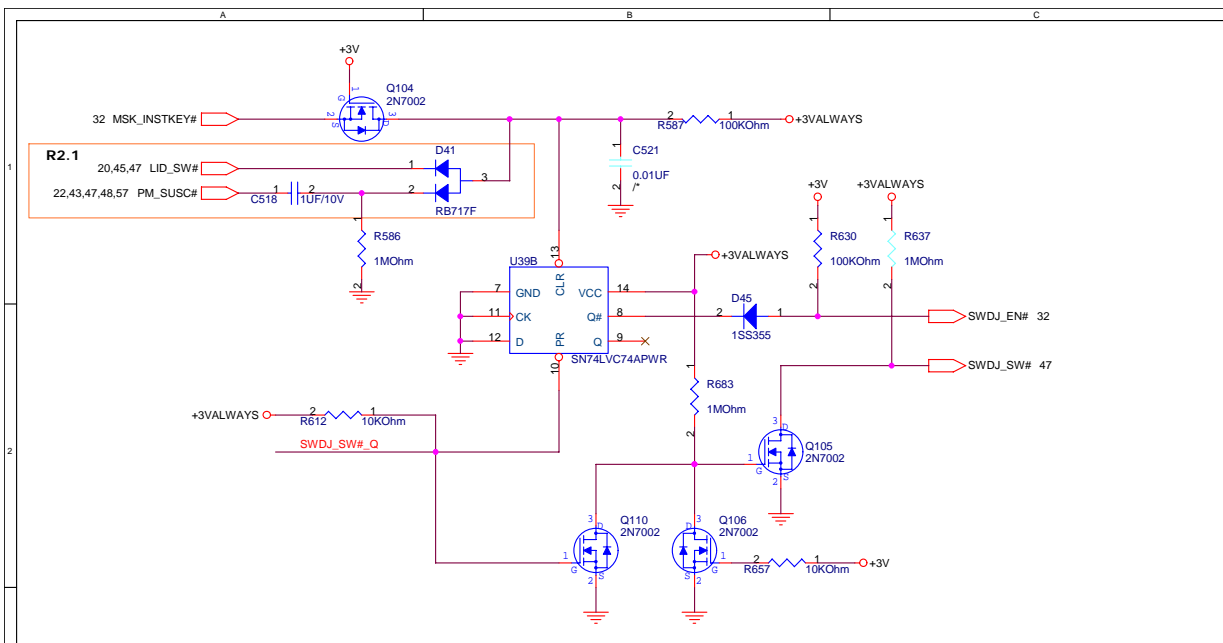
1394A CON



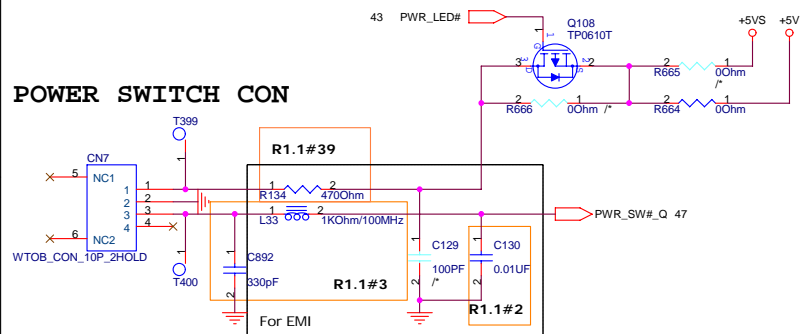
To solve MS-Duo short with SD card



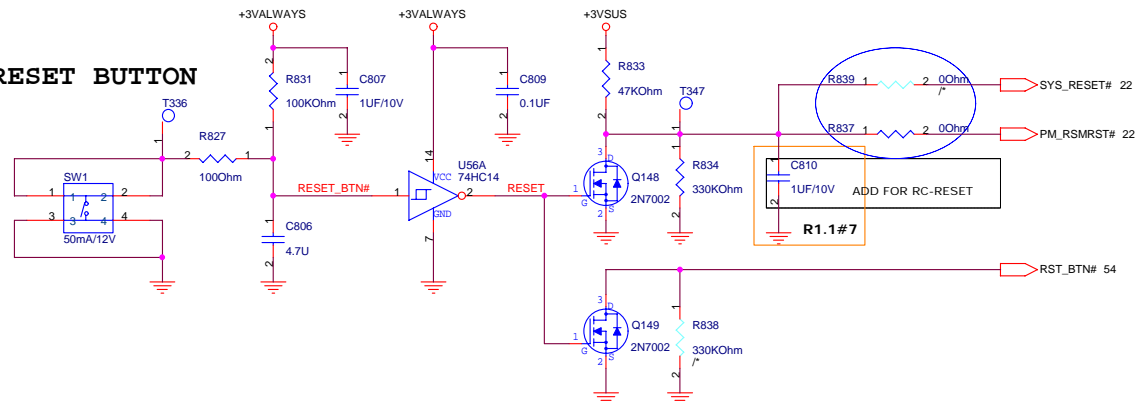
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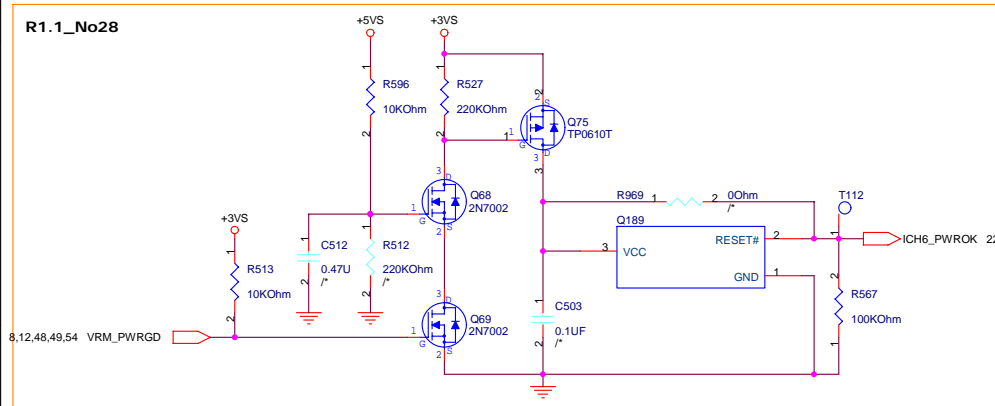
POWER SWITCH CON



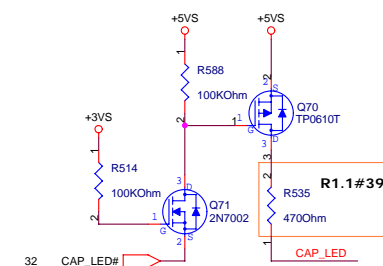
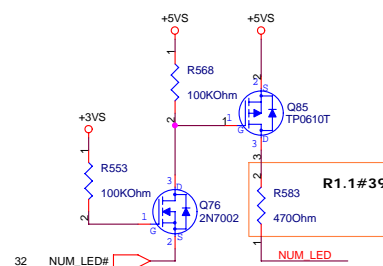
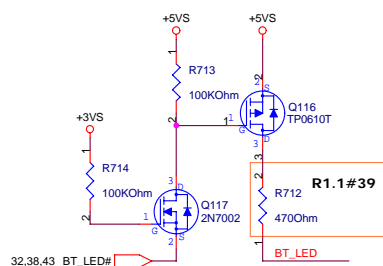
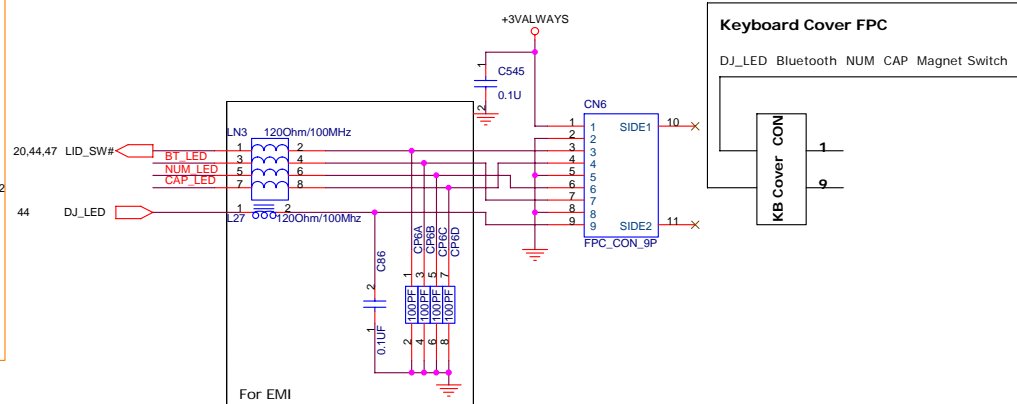
RESET BUTTON



R1.1_No28

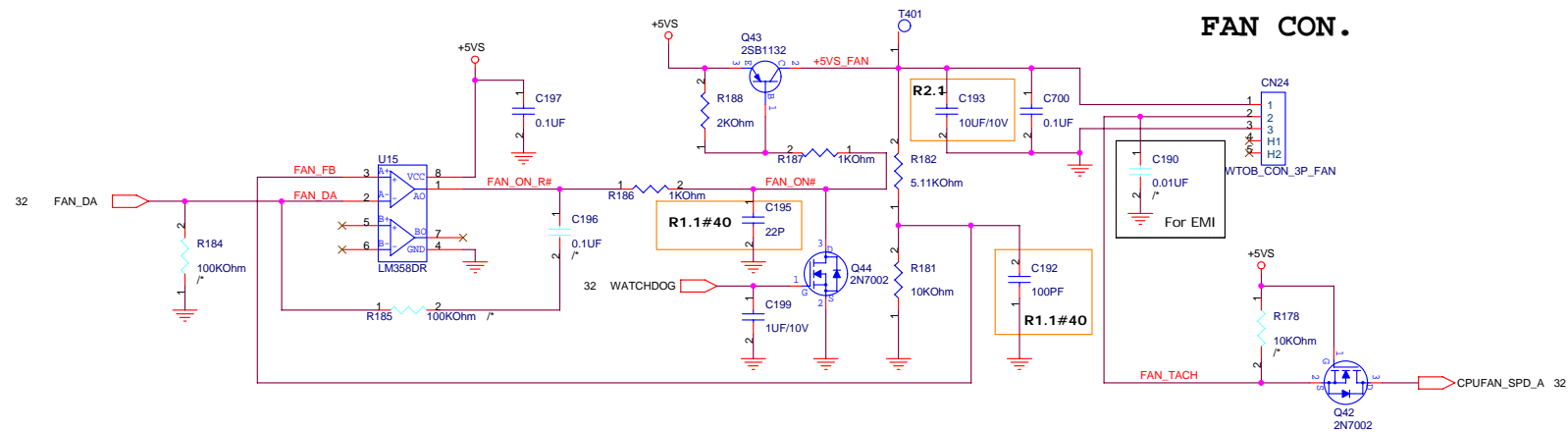


KB COVER CON



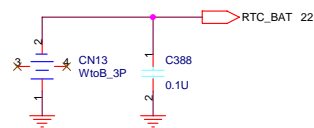
bom

 PROJECT: W3V	REVISION 2.1	DATE: Monday, January 17, 2005 SHEET 45 OF 63	DESCRIPTION: PWR SW / RESET / KBC LEDs	SCHEMATIC FILE NAME: <OrgName> RELEASE DATE:	DESIGN ENGINEER: M.Y.
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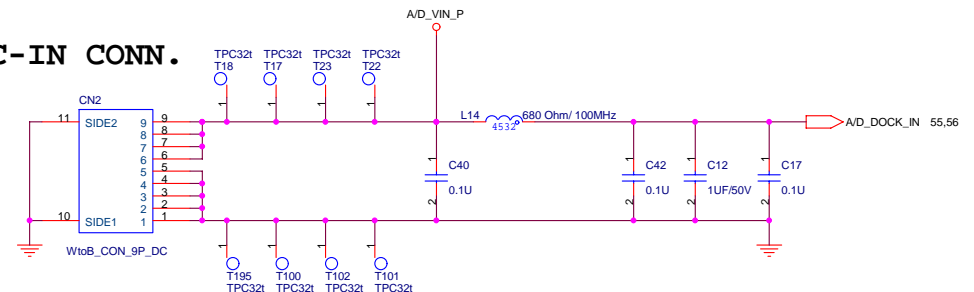
FAN CONTROL

RTC BAT CON.



RTC Battery
P/N=07-016322032

DC-IN CONN.



bom



PROJECT: W3V

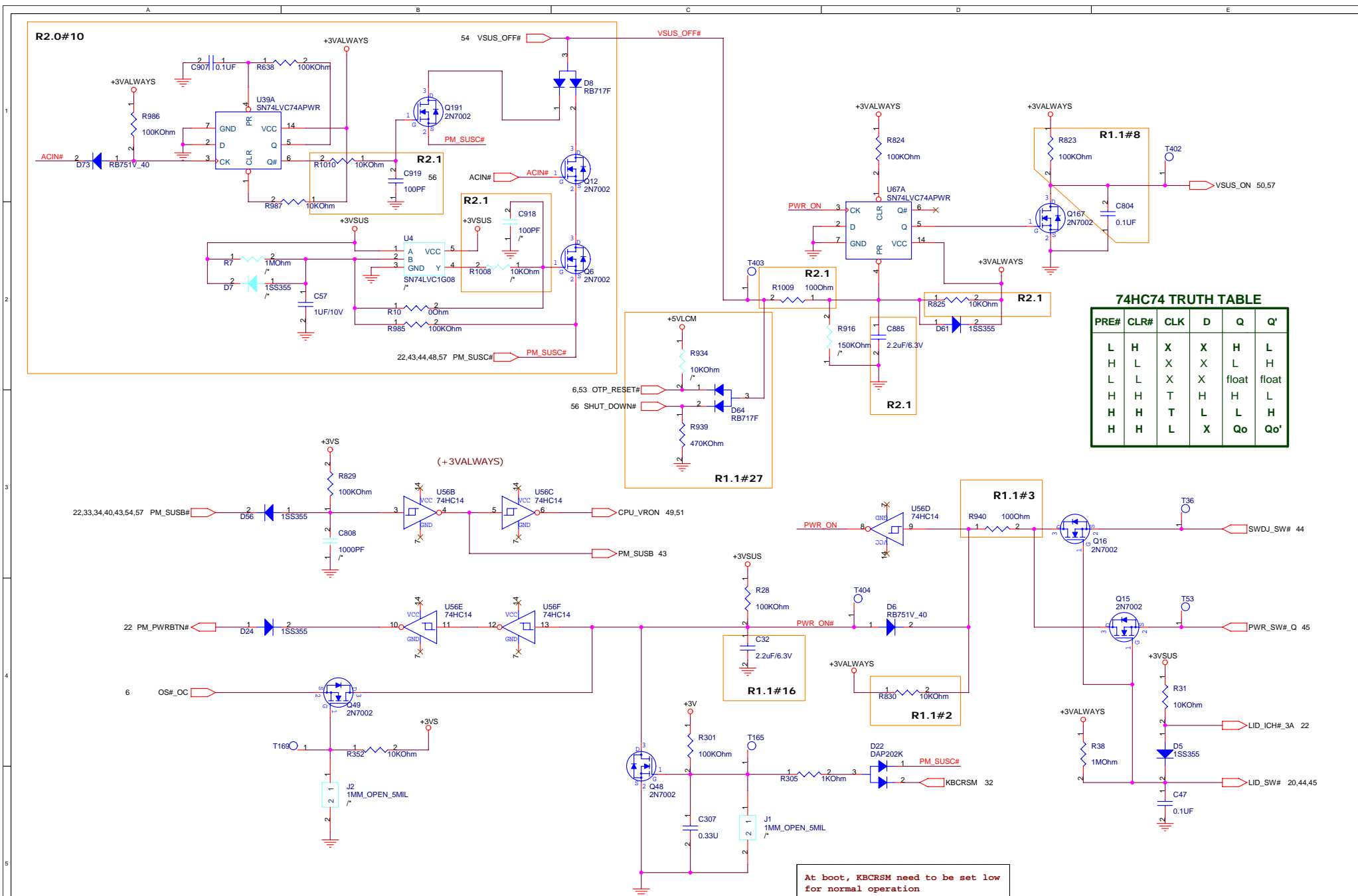
REVISION
2.1

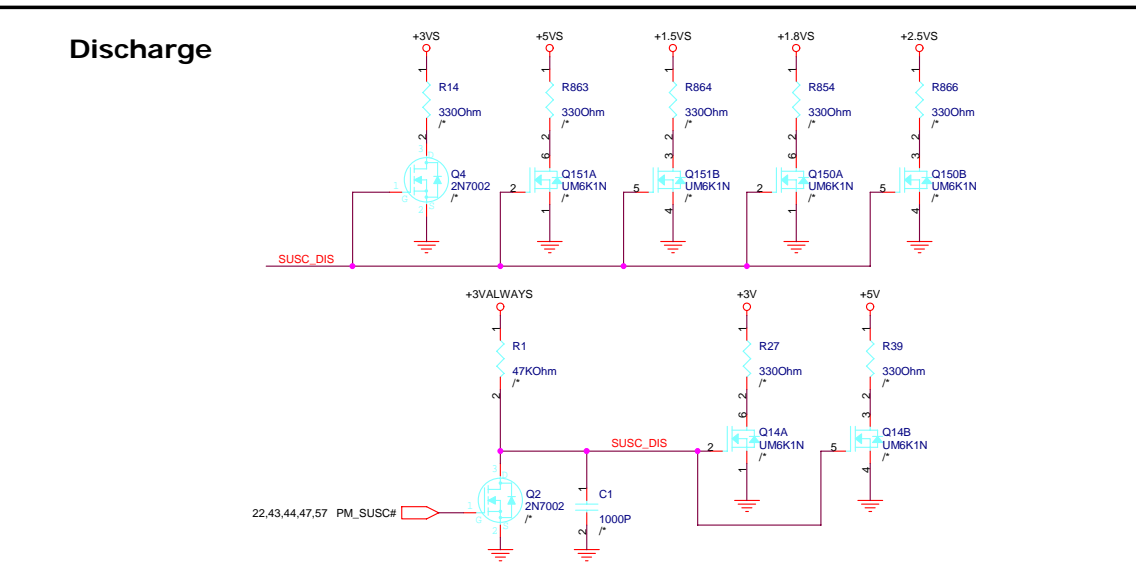
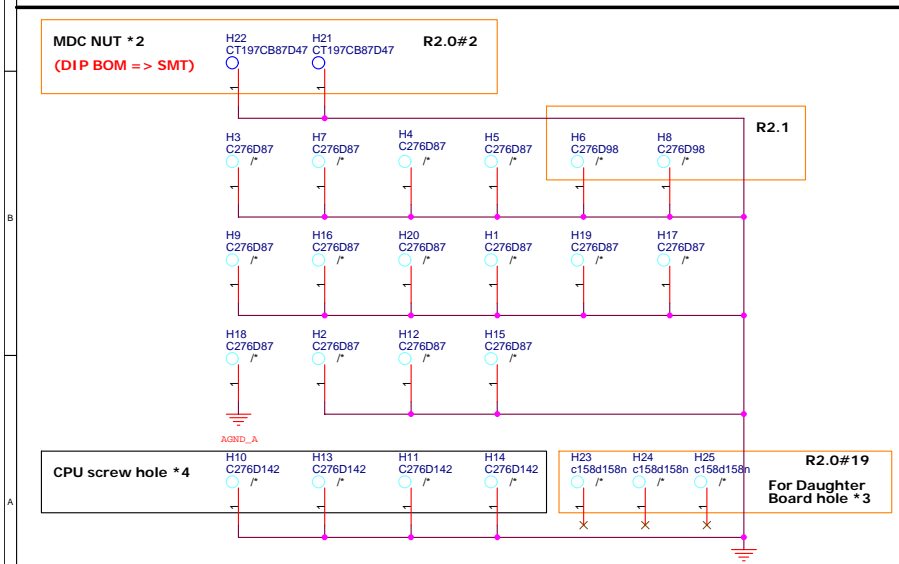
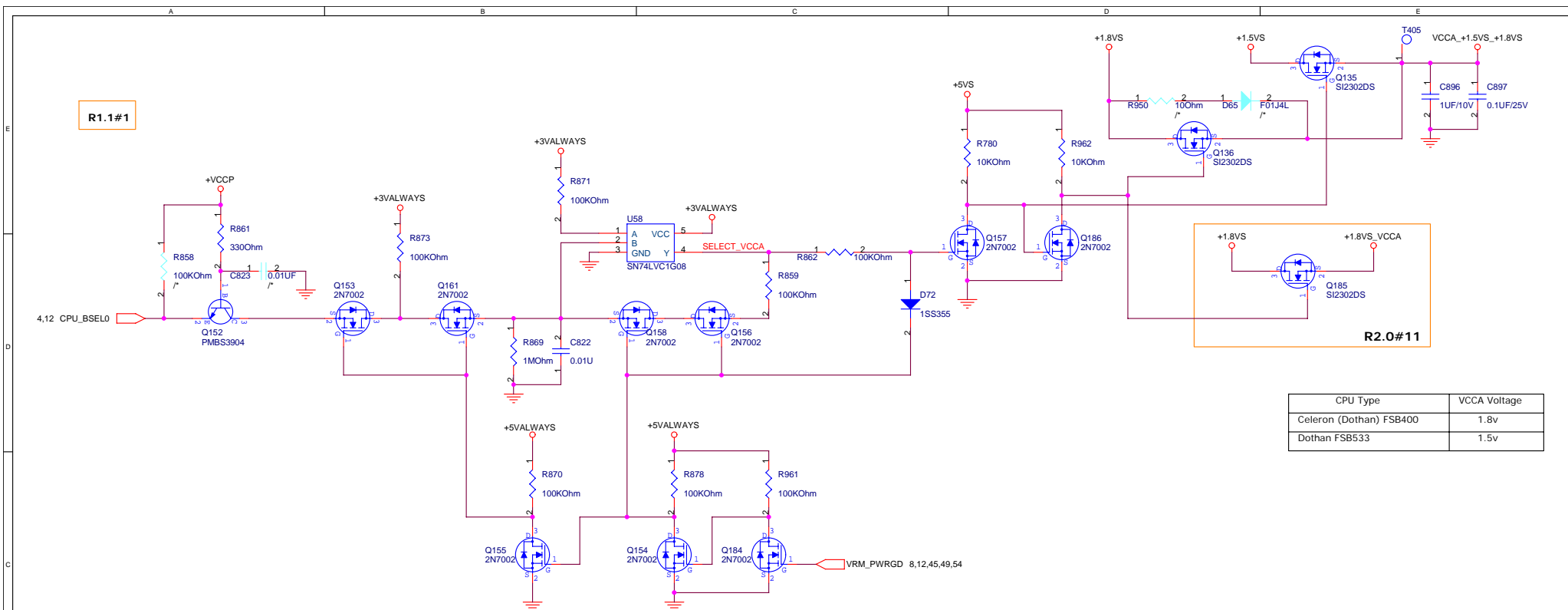
DATE: Monday, January 17, 2005
SHEET 46 OF 63

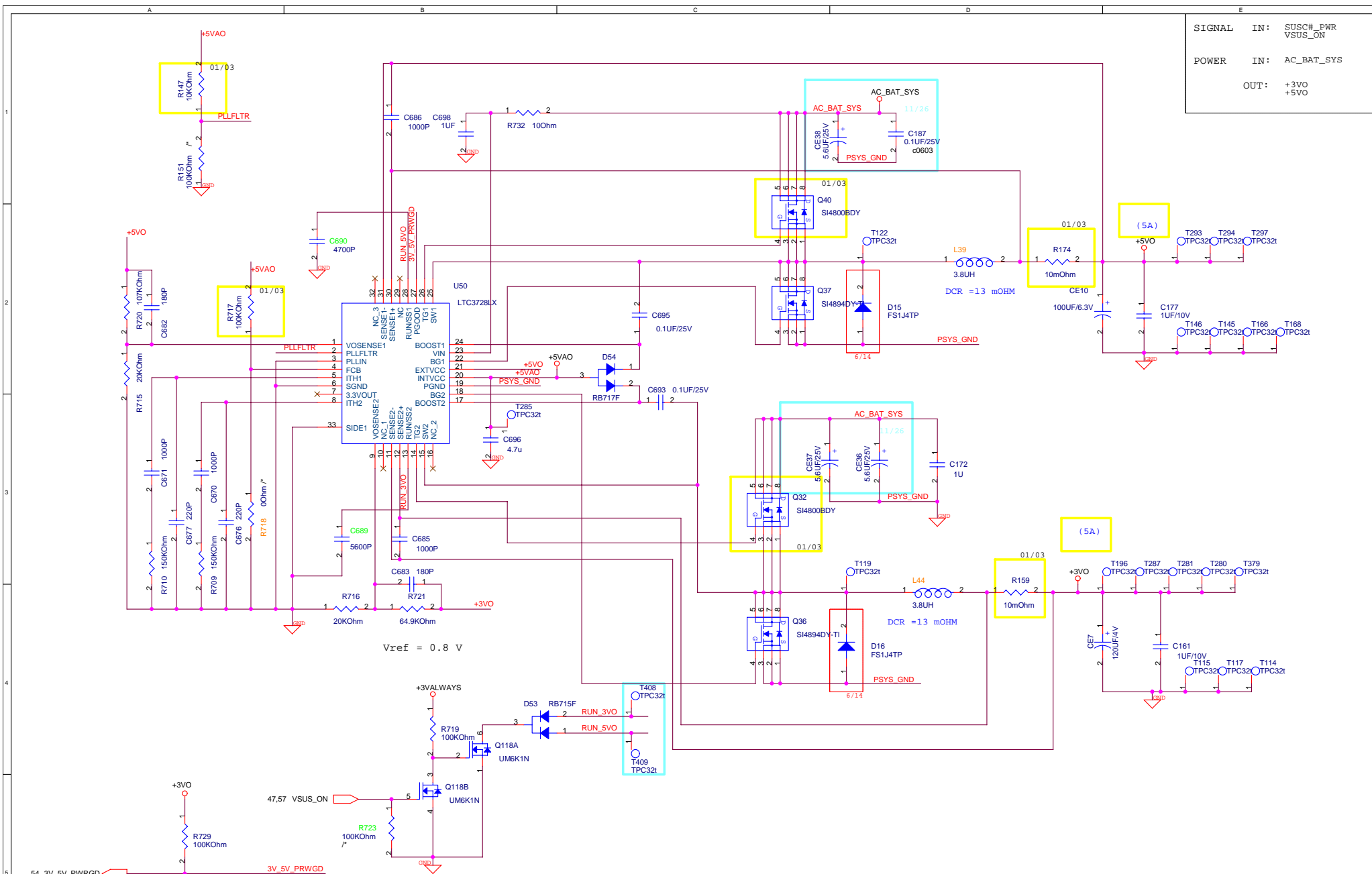
DESCRIPTION:
FAN / RTC / DC_IN

SCHEMATIC FILE NAME : <OrgName>
RELEASE DATE :

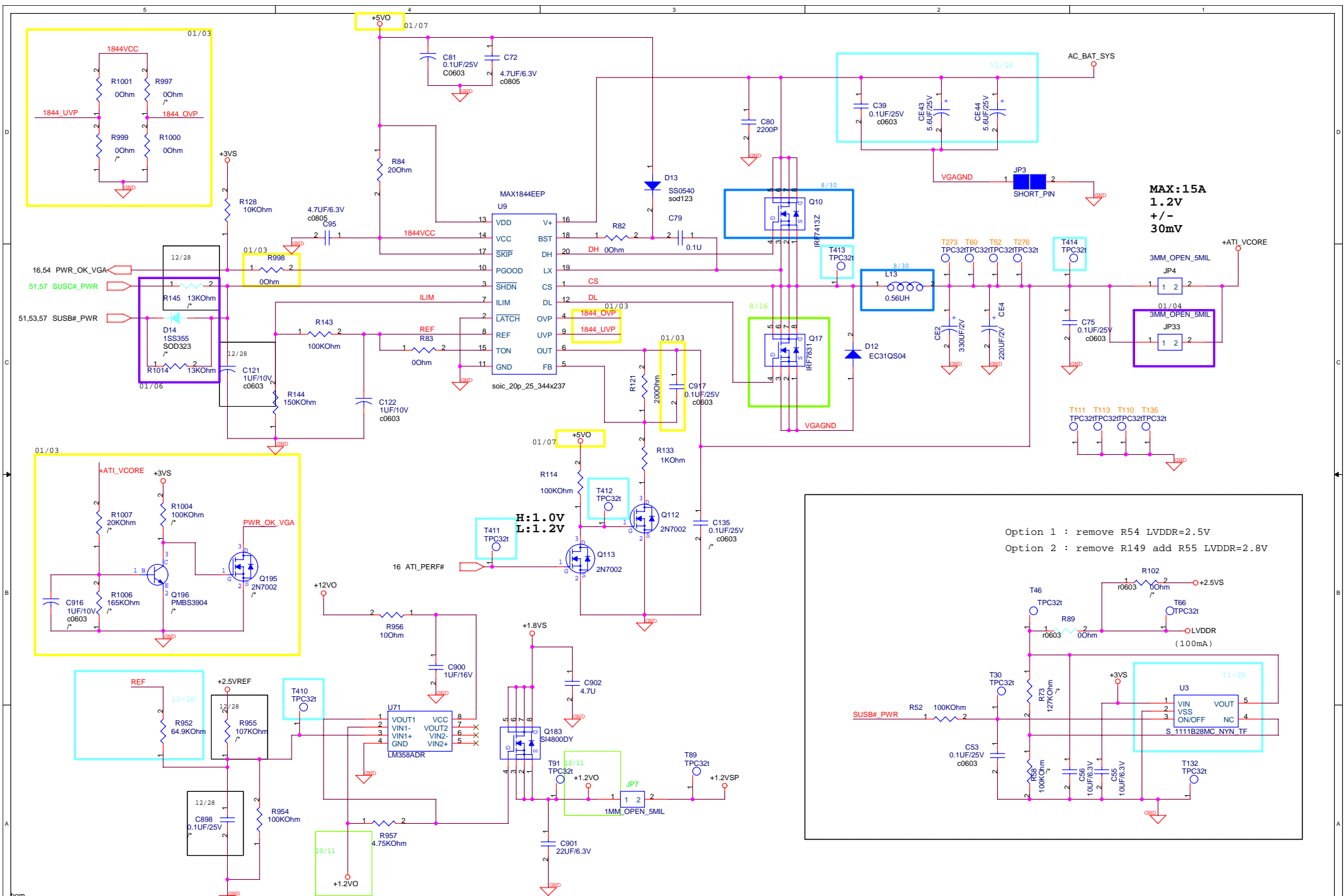
DESIGN ENGINEER :
M.Y.



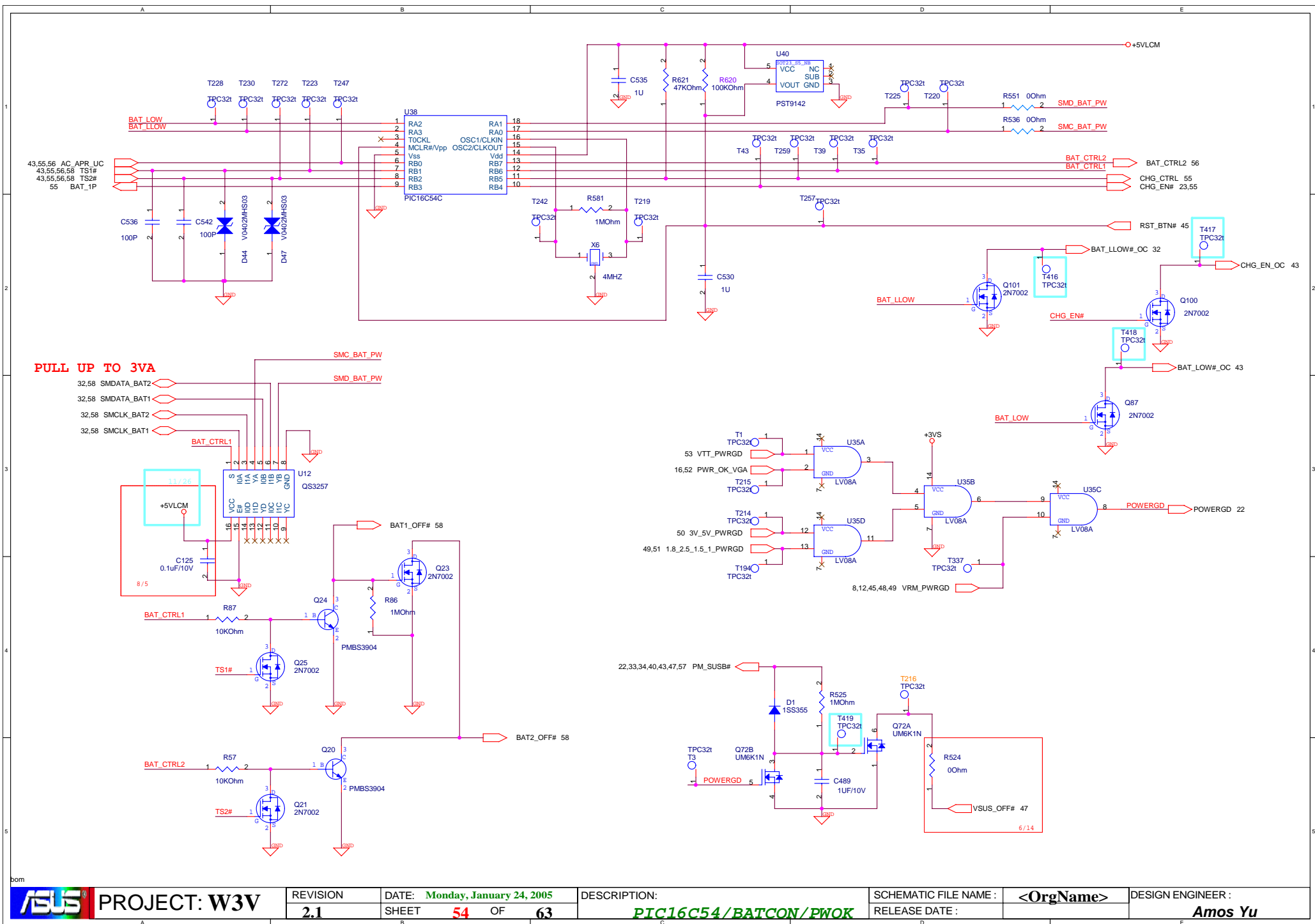




SIGNAL	IN:	SUSC#_PWR
		VSUS_ON
POWER	IN:	AC_BAT_SYS
	OUT:	+3VO
		+5VO













Revision History

R1.1

SYSTEM

1. (p48) Modify CPU +VCCA
2. (p45,47) Fix auto power on when AC in in AC mode
3. (p45,57) Solve U56 easily damaged
4. (p8) Add R941 for BIOS internal VGA strapping
5. (p8) U48, D30 change from ICH6_PWROK to VRM_PWRGD (p12) R363 change to 10K, C893=0.47uF
6. (p20) Fix PID1 can't strapped low
7. (p45) Modify power sequence of +3VSUS -> PM_RSMRST#
8. (p47) Fix that +3VSUS/+5VSUS may be turned on for a while when the power comes in at the first time
9. (p16) Fix TV out can't work
10. Add Bluetooth support
11. (p24) DEL reserved V5REF_SUS circuit
12. (p12) ADD net "CPUSELO/1" for layout
13. (p37) Change X7 part
14. (p23) Add R949 to reduce overshoot
15. (p34) Solve pop noise in Windows boot
16. (p47) Power button debounce
17. Tune X'tal freq. (p22) C353/C356 (p26) C350/C354 (p32) C78/C93 (p41) C355/C360
18. (p27) Change CN32 part
19. (p43) Change R924 to +5VLCM to solve +5V leakage in power off.
20. (p20) Tune LCD_VCC timing
21. (p44) Modify CN10 pin define for ID change
22. (p23,34) Add ALC861VS PC-Beep support
23. (p33) ADD T388, U61.3 ADD "AUD_GPIO0" (p34) DEL R482, ADD U72
24. (p34,35) DEL net "MIC_AGND_A"
25. (p39) ADD voltage divider for Mic VREF
26. (p34) for EMI request
27. (p47) VSUS_OFF#
28. (p45) Modify power on sequence
29. (p43,p32) Reserved for bluetooth LED
30. (p39) Reserved PCI_INTC# for MINI-PCI.
31. (p29) Solve USB power surge warning when USB HDD plug-in
32. (p28) Support CSEL+ ODD
33. (p6) GMCH_THRMTRIP# no function in high temperature
34. (p10) unstuff for W3V
35. (p17) Adjust ATI 27MHz Vhigh
36. (p23) Aviod logic output unstable
37. (p4) Fix BT_VCC unstable
38. (p40) Tune clock timing
39. (p43) Tune LED current for LED spec
40. (p46) Adjust for +5VS_FAN stable
41. (p47) Fix can't power on in battttery mode

POWER

- 1 (p49) Add R942, MCH_OK connect to 1.8_2.5_1.5_1_PWRGD, C248, R233 unstuff

R2.0

SYSTEM

1. (p20) Adjust BACK_EN Vhigh
2. (p48) Change MDC nut
3. (p22,38,43) DEL BT_ON#, control BT_VCC by BT_LED#
4. (p29) Adjust for USB-IF spec
5. (p32) Solve SMBus loss pull-high power in power-off.
6. (p23) Reduce PCI_RSTNS# overshoot
7. (p23) Reduce 2V step on PCI_RST#
8. (p12) Tune W3V clock
9. (p25) Update PCB_VID
10. (p47) Solve system can't power on in battery mode
11. (p48) Modify +1.8VS_VCCA gate ckt
12. (p20) Avoid U28 damage
13. (p34) Remove reserved Windows de-pop Ckt
14. (p16) Tune W3A HSYNC/VSYNC timing
15. (p21) Tune W3V HSYNC/VSYNC timing
16. (p28) Modify for swap bay detection.
17. (p34) For EMI
18. (p20) For EMI
19. (p48) For PD4
20. (p21) For ME
21. (p33) DEL net "AUD_GPIO0"

bom



PROJECT: W3V

REVISION

2.1

DATE: Wednesday, January 26, 2005

SHEET

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OF

63

DESCRIPTION:

History

SCHEMATIC FILE NAME :

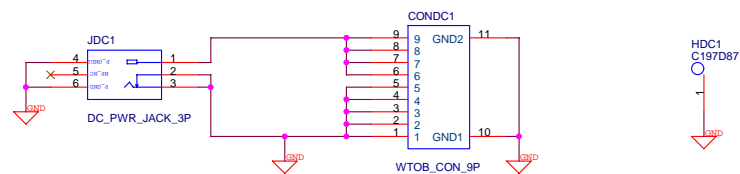
<OrgName>

DESIGN ENGINEER :

Alice Shih

RELEASE DATE :

DC IN

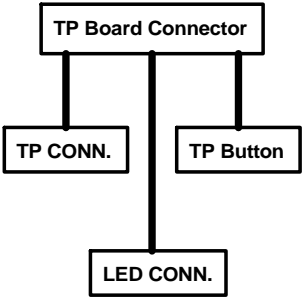


bom

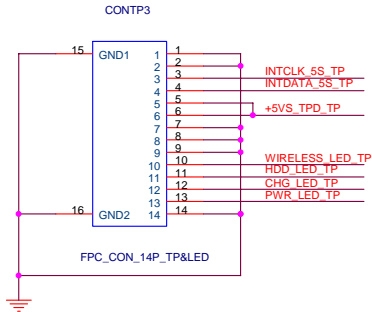
	PROJECT: W3V	REVISION 2.1	DATE: Wednesday, January 26, 2005 SHEET 61 OF 63	DESCRIPTION: DC_IN CONNECTOR	SCHEMATIC FILE NAME : RELEASE DATE :	<OrgName>	DESIGN ENGINEER : Renyu Wang
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W3V TP & LED Board

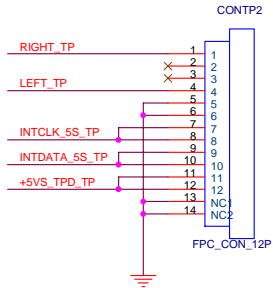
Block Diagram



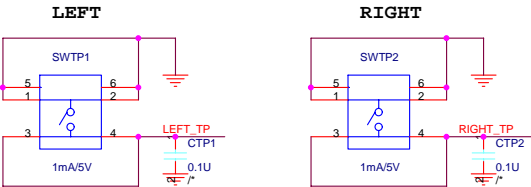
TOUCHPAD & LED BOARD CONN.



TP CONN.



TOUCHPAD BUTTON



LED CONN.

